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Digital Phase Lock Loops

Architectures and Applications

Springer

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by

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Contents

Preface

Since their introduction by de Bellescize in 1936, analogue Phase-Locked Loops (PLLs) have continued to play a major role in the advancement of several fields such as communications, signal processing and control [11]. Despite their performance advantages, analogue PLLs suffer from major drawbacks related to their analogue nature. These include aging and temperature drift effects, the sensitivity to component tolerances and operating conditions. In an attempt to combat the aforementioned drawbacks, Digital Phase-Locked Loops (DPLLs) were introduced in the 1970s as a result of the advent of digital technology and the urgent need for robust methods of synchronization for space communications [12]. One of the most promising versions of the DPLL is the Digital Tanlock Loop(DTL), which was introduced [13]. This loop offered many appealing features such as the linearity of the phase characteristics and the insensitivity to the variations in signal power. However, it did not gain a lot of popularity due to the complexities faced in the design of the Hilbert transformer, one of its major components.

Recently, an approach was proposed to rid the DTL from the Hilbert Transformer and its complexities by replacing it with a fixed time delay unit. This approach preserves most of the desirable characteristics of the DTL except for the linearity. The loop was named the Time Delay Digital Tanlock Loop (TDTL) [71].

Motivated by the desirable features of the TDTL, this book aims at analyzing the performance of the TDTL and implementing it as a reconfigurable system, which will serve as a testbed for future experimentations. The flexibility offered by reconfigurable computing devices, especially Field Programmable Gate Arrays (FPGAs), is being utilized in most communication systems to implement complex high-speed algorithms [14]. In addition to that, it will facilitate in upgrading and modifying of the TDTL testbed with minimum effort and complexity.

FPGAs are on the verge of revolutionizing digital signal processing in the manner digital signal processors did two decades ago. This is expected since FPGAs offer various attractive features such as rapid prototyping, on-the-fly

upgradeability, code reuse and reduction in size and power consumption [14, 15].

The Main Contributions

The main contribution offered by this book is the introduction of modified architectures of the newly proposed TDTL that overcome the inherent limitations of the loop and undermines the tradeoffs between the locking range and speed of acquisition requirements. The proposed architectures are purely digital, therefore lending themselves to the implementation using reconfigurable modules without a significant increase in the complexity of implementation or design procedures.

Another major contribution offered is what may be considered as the first documented implementation of the TDTL using FPGAs. The implemented system will serve as a testbed for the performance enhancement and optimization of the loop.

Organization of Book

The first chapter provides a general review of phase-lock loops. Chapter two reviews the uniform and non-uniform type Digital Phase Lock Loops (DPLL). Chapter three covers the Time Delay Digital Tanlock Loop (TDTL) and it's convergence behavior. The following two chapters will focus on the Hilbert Transformer and Time-Delay, and the analysis of the TDTL in noise. The sixth chapter will cover the analysis, modified architectures, and the simulation results of the various TDTL architectures for improved performance. Chapter seven documents the design and implementation of a reconfigurable TDTL system using Field Programmable Gate Arrays, and analyzes the acquired results. Finally, chapter eight covers selected applications of the TDTL.

About the Authors

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Prof. Al-Araji received the B.Sc., M.Sc., and Ph.D. degrees from the University of Wales Swansea, (UK), all in electrical engineering in 1968, 1969, and 1972 respectively. Since September 2002, Professor Al-Araji was appointed Professor

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Zahir M. Hussain took the first rank in Iraq in the General Baccalaureate Examinations 1979 with an average of 99%. He received the B.Sc. and M.Sc. degrees in electrical engineering from the University of Baghdad, Iraq, in 1983 and 1989, respectively, and the PhD degree in electrical engineering from Queensland University of Technology (QUT), Brisbane, Australia in 2002. He has over 15 years of experience in teaching and research in various universities. He worked in several projects including the EEG biomedical project at QUT (1999-2001), where he contributed to solving the problem of instantaneous frequency estimation of multicomponent signals. In July 2001 he joined the School of Electrical and Computer Engineering, RMIT University, Melbourne, Australia as a Research Fellow in a 3G commercial project, then Lecturer of Signal Processing and the academic leader of another 3G communications project in November 2001. In March 2002 he was promoted to Senior Lecturer. In November 2005 he was promoted to Associate Professor and received the RMIT Publications Award. Since 2001, he has been the principal supervisor of nine PhD students; six of them have recently completed their studies successfully. Dr. Hussain is the author/co-author for over 120 technical papers on various fields. His current research interests are signal processing, communications,

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Dr. Mahmoud Al-Qutayri received the B.Eng. degree in electrical engineering from Concordia University, Quebec, Canada, in 1984, the M.Sc. degree in electronic engineering from Manchester University, UK, in 1987, and the Ph.D. degree in electronic engineering from University of Bath, UK, in 1992. He has over fifteen year of experience in teaching and research at various universities. From 1988-1992 he was a research officer at the University of Bath, UK were he worked on testing techniques for analogue and mixed-signal integrated circuits. The project was in collaboration with another two universities and an integrated circuits design company. Dr. Al-Qutayri has also carried out consultancy work for a number of companies including ViewLogic, Lucas, Gent, Philips and others. From 1992-1996 he was a Senior Lecturer at DeMontfort University, Leicester, UK. He subsequently joined Etisalat (Telecommunications) University College in the UAE where he is currently an Associate Professor in the Department of Electronic Engineering. His research interests include testing and design for testability of mixed-signal integrated circuits, and application of reconfigurable computing to signal processing and communication systems, steganography and steganalysis. He published over forty technical papers in international journals and conferences. He is a reviewer to a number of international conferences and journals, and is involved in the organization of a number of international conferences in various capacities. Dr. Al-Qutayri is a Senior Member of the IEEE, member of the IEE and Chartered Engineer (Ceng.) in the UK. His e-mail address is: mqutayri@euc.ae.

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Acronyms

ADC	analog-to-digital converter
CDTL	conventional digital tanlock loop
CR	Cramer-Rao (bound)
DCO	digital controlled oscillator
DPLL	digital phase-locked loop
DTL	digital tanlock loop
FIR	finite impulse response
FM	frequency modulated signal
FT	Fourier transform
HT	Hilbert transformer
IF	instantaneous frequency
i.i.d.	independent and identically distributed
PLL	phase-locked loop
MSB	most significant bit
PDF	probability density function
PED	phase error detector
SNR	signal-to-noise ratio
TDTL	time-delay digital tanlock loop
var	variance
VCO	voltage controlled oscillator
ZC-DPLL	zero-crossing digital phase-locked loop
VD-TDTL	variable delay TDTL
SS-ATDTL	sample sensing adaptive TDTL
EES-ATDTL	early error sensing adaptive TDTL
ATDTL	adaptive TDTL
VO-TDTL	variable order TDTL

Chapter 1

General Review of Phase-Locked Loops

1.1 Overview of Phase-Locked Synchronization Schemes

Although not explicitly stated, the presence of transmitter-receiver synchronization is usually assumed in analyzing the performance of communication systems. For example, in the case of coherent Phase-Shift Keying (PSK) demodulation, the receiver is required to perform maximum-likelihood symbol decisions by comparing the incoming signals with a set of internally-generated reference signals. Generating these reference signals, which are assumed to be identical to those of the signaling alphabet at the transmitter, requires the receiver to be synchronized with the received carrier. This means that the there has to be phase alignment between the incoming carrier and the generated replica at the receiver, and therefore, the incoming carrier and the replica in the receiver would pass through zero simultaneously if there were no information modulated on the incoming carrier. The receiver in this state is said to be in phase-lock with the transmitter, and this condition must be closely approximated if coherently modulated signals are going to be accurately demodulated [6, 80].

Being in phase-lock means that the receiver's local oscillator is synchronized in both frequency and phase with the received carrier. In addition to that, phase-lock must also be established with the received subcarriers if the information-bearing signal is not modulated directly on the carrier. If the carrier and subcarrier are not kept in phase concurrence by the transmitter, the receiver is required to generate a replica of the subcarrier and control it's phase separately from that of the carrier replica, and therefore, enabling the receiver to achieve phase-lock on both the carrier and subcarrier [5].

The receiver is also required to achieve Symbol Synchronization by tracking the start and end of incoming symbols. These are required to determine the proper intervals for integrating the energy of symbols, and ensure making correct symbol decisions. This is achieved by producing a square wave whose zero transitions are aligned with the incoming signal's transitions between symbols in order to reach a symbol-lock state. The typically large number of carrier cycles per symbol period necessitate that achieving this level of synchronization with different circuitry than that used for phase synchronization [6, 7].

In the context of communication systems, synchronization is also required in a higher level, namely frame synchronization. Since information is usually organized into blocks, which are coded for forward error control and multiple access purposes, the knowledge of the boundaries between code words must be available at the decoder to ensure correct message or data extraction. In Time Division Multiple Access (TDMA), where multiple users are time-sharing common channels, it is necessary to know where the boundaries between channel users are in order to distribute the information appropriately. Similar to symbol synchronization, frame synchronization is equivalent to being able to generate a square wave at the frame rate, with the zero crossings matching the transitions from one frame to the next [6, 7].

All levels of synchronization, namely phase, symbol and frame, are required in most digital communication systems employing coherent modulation techniques. Conversely, noncoherent-modulation-based system usually make use of symbol and frame synchronization, and another level called frequency synchronization, in which the replica of the carrier generated by the receiver is allowed to have an arbitrary constant phase offset from the received carrier. The choice between coherent and noncoherent modulation methods is governed by the desired performance and complexity of implementation [80].

Although so far it seems that the synchronization is related only to the receiver, there are some communication systems that utilize the transmitter in performing a great deal of the synchronization role by tuning the timing and frequency of its transmissions to match the expectations of the receiver. For example, many terrestrial terminals in satellite communication networks are directing their transmissions toward a single satellite receiver. These transmitters rely on the receiver return paths to determine the accuracy of their synchronization, and therefore, transmitter synchronization often implies two-way communications or a network in order to be successful. Thus, transmitter synchronization is often called network synchronization [6].

1.2 The Synchronization Challenge

As mentioned earlier, there is a compromise between the performance and the implementation complexity. Extra levels of synchronization come at the cost of additional hardware or software in the receiver for acquisition and tracking. There are also costs associated with the synchronization overhead, energy and power consumption. However, the outcome of improved performance and versatility still outweighs the aforementioned costs, and communications system designers are always oriented towards designing systems with high degree of synchronization [7].

An example of this design strategy is the case of commercial analogue radio broadcast employing Amplitude Modulation (AM). This system is usually comprised of a central transmitter serving multiple receivers within its coverage area, and involves no synchronization. However, the passband of the receiver must be wide enough to house the modulating (information-bearing) signal, and account for its abrupt shifts in frequency due to the fluctuations in the output frequency of the local oscillator generating the carrier [6]. With this extra requirement, the performance of the receiver will degrade due to the fact that extra noise energy will be passed to the detector, which was not accounted for in the theoretical analysis. Adding the element of synchronization to this receiver will solve the problem, and improve the performance considerably. If the receiver contains extra circuitry for tracking the incoming carrier, the receiving filter will be centered about the carrier even if it fluctuates, and the detected noise energy will be decreased leading to a lower signal-to-noise-ratio (SNR) [6].

Moving to the digital communications domain, the same compromise can be demonstrated in the choice of modulations schemes. For example, noncoherent Binary Frequency Shift-Keying (BFSK) is considered among the simplest digital receivers in terms of implementation, requiring only symbol and frequency synchronization. However, choosing this modulating scheme will result in a 4-dB penalty in terms of bit error performance, i.e. the more complex coherent BPSK receiver can achieve the same bit error probability with 4 dB less SNR [7]. The trade-off between complexity and performance is further extended with the use of error-control coding algorithms. While they offer better performance under stringent operating conditions, they also result in more complex implementations, and require higher levels of synchronization between blocks, messages, and frames [81, 80]. Having discussed the principles and levels of synchronization, and the trade-offs between implementation costs and performance, the next section will explain the basic building block of almost all synchronization systems, namely the Phase-Locked Loop (PLL).

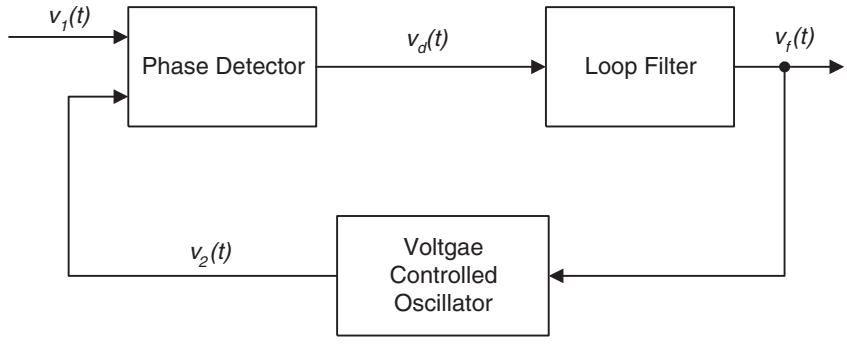


Figure 1.1: Block Diagram of the PLL.

1.3 Phase-Locked Loops

The PLL represents one of the most active topics in signal processing and communication theory. The initial ideas started as early as 1919 in the context of synchronization of oscillators. The theory of phase-locked loop was based on the theory of feedback amplifiers. The PLL contributed significantly to communications and motor servo systems. Due to the rapid development of integrated circuits (IC's) since the 1970's, PLLs are widely used in modern signal processing and communication systems, and it is expected that PLL will contribute to improvement in performance and reliability of future communication systems. The applications of PLLs include filtering, frequency synthesis, motor-speed control, frequency modulation, demodulation, signal detection, frequency tracking and many other applications [1, 9, 10, 11].

1.3.1 Analog Phase-locked Loops

A PLL is defined as a circuit that enables a particular system to track another one. More precisely, a PLL is a circuit synchronizing an output signal (generated by an oscillator) with a reference or input signal in the frequency as well as in phase [5].

In the synchronized or the locked state, the phase error between the oscillator's output and the reference signal is either zero or an arbitrary constant. In the case of a phase error building up, the oscillator is tuned by a control mechanism in order to reduce the phase error to a minimum. In such a control system, the phase of the output signal is actually locked to the phase of the reference input. This is the reason behind calling this specific control system a Phase-Locked Loop [5]. The basic functional components of a PLL are: A voltage controlled oscillator (VCO), A phase detector (PD), and A loop filter (LF).

The signals of interest in the PLL block diagram shown in Figure 1.1 are defined as follows: The reference (or input signal) $v_1(t)$ with an angular frequency ω_1, The output signal $v_2(t)$ of the VCO with an angular frequency ω_2, The output signal $v_d(t)$ of the phase detector, The output signal $v_f(t)$ of the loop filter, and The phase error θ_e, defined as the phase difference between signals $v_1(t)$ and $v_2(t)$.

The VCO oscillates at an angular frequency ω_2 which is determined by the output signal v_f of the loop filter. The angular frequency ω_2 is given by

$$\omega_2(t) = \omega_o + K_o v_f(t) \tag{1.1}$$

Where ω_o is the centre frequency of the VCO and K_o is the VCO gain. The PD compares the phase of the output signal with the phase of the reference signal and generates an output signal v_d that is approximately proportional to the phase error θ_e, the former signal is given by:

$$v_d(t) = K_d \theta_e, \quad \theta_e \to 0 \tag{1.2}$$

where K_d represents the gain of the PD. The output signal $v_d(t)$ consists of a dc component and a superimposed ac component. Since the latter is undesired, it is cancelled by the loop filter. Assuming the angular frequency of the input signal $v_1(t)$ is equal to the centre frequency ω_o, the VCO then operates at its centre frequency ω_o, and the phase error is zero, indicating the output signal of the loop filter v_f is also zero. If the phase error θ_e was not initially zero, the PD would develop a nonzero output signal v_d. After some delay the loop filter would also produce a finite signal v_f, which will cause the VCO to change its operating frequency in such a way that the phase error finally vanishes.

Now, assume that the frequency of the input signal is changed suddenly at a time instant t_o by the amount of $\Delta\omega$. This will cause the phase of the input signal to lead the phase of the output signal, and a phase error will build up and increase with time. The PD develops a time-increasing signal $v_d(t)$, which will cause $v_f(t)$ to rise after some delay introduced by the loop filter. This causes the VCO to increase its frequency in order to minimize the phase error, and after some settling time the VCO will oscillate at a frequency that is exactly the frequency of the input signal. Depending on the type of the loop filter used, the final phase error will have been reduced to zero or to a finite value.

The VCO now operates at a frequency that is greater than its center frequency ω_o by an amount $\Delta\omega$, this will force the signal $v_f(t)$ to settle at a final value of $v_f = \Delta\omega/K_o$. If the centre frequency of the input signal is frequency modulated by an arbitrary low-frequency signal, then the output signal of the loop filter is the demodulated signal. The PLL can consequently be used as an

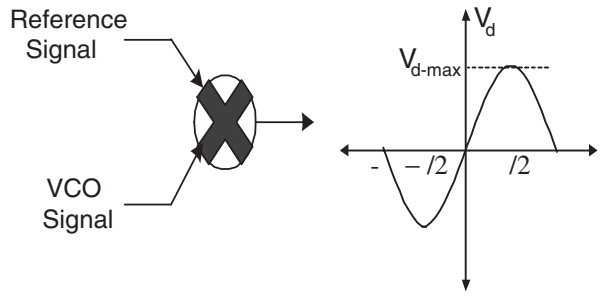


Figure 1.2: Classical Mixing Phase Detector.

FM demodulator, or in more general terms, it can be used as a demodulator of any scheme that stores the information in the frequency of the phase of the modulated carrier [5].

One of the most interesting capabilities of the PLL is its ability to suppress noise superimposed on its input signal. Assuming that the input signal of the PLL is degraded by noise, the PD will attempt to measure the phase error between the input and output signal. The noise at the input causes the zero crossings of the input signal $v_1(t)$ to be advanced or delayed in a stochastic manner, causing the PD output signal $v_d(t)$ to jitter around an average value.

If the cut-off frequency of the loop filter is low enough so that almost no noise will be noticeable in the signal $v_f(t)$ and the VCO will operate in such a way that the phase of the signal $v_2(t)$ is equal to the average phase of the input signal $v_1(t)$, it can be stated that the PLL is able to detect a signal that is badly degraded by noise. These simplified considerations show that the PLL is a typical servo system that controls the phase of the output signal $v_2(t)$ [1, 5].

1.3.2 PLL Basic Components

The Phase Detector

As previously mentioned the function of the phase detector block is to compare the phases of the input and output signals and generate an error signal proportional to the phase deviation between them. The most prevalent device capable of achieving this function is the mixer, which generates the sums and differences of the frequencies at its input terminals.

The mixing phase detector shown in Figure 1.2 will be discussed later in Section 1.3.3. This PD has a superior noise performance to all the other detectors,

due to the fact that it operates on the entire amplitude of the input and VCO signals, rather than quantizing them to 1 bit [12]. Balanced mixers are best suited for PLL applications in the microwave frequency range as well as in low noise frequency synthesizers. However, this results in a loop whose gain is dependent upon the signal amplitude. Furthermore, nonidealities in the circuit implementation of the mixer result in nonlinear responses. When noise is not an issue, it is advantageous to move to a detector that has immunity to these effects [1, 2, 3, 4].

The Voltage-Controlled Oscillator

The actual clock generated by a PLL comes from the voltage-controlled oscillator (VCO), which generates a periodic oscillation. The frequency of this oscillation can be controlled by modulating some control voltage. In a PLL, the control voltage corresponds to some filtered form of the phase error. In response to this, the VCO adjusts its frequency. As the VCO frequency is slewed by the control voltage, the phase error is driven towards zero. This frequency adjustment to achieve phase lock results in the model of a VCO as an integrator [1, 5].

VCOs are generally of the form of a ring oscillator, relaxation oscillator or a resonant oscillator. The ring oscillator takes the form of an odd number of inverters connected in a feedback loop. The relaxation oscillator uses a Schmitt-trigger to generate a stable square wave [2]. The latter puts a resonant circuit in the positive feedback path of a voltage to current amplifier as shown in Figure 1.3. The resonant circuit in the positive feedback path has poles close to the $j\omega$ axis. Consider the bandpass filter:

$$F(s) = \frac{2\zeta\omega_o s}{s^2 + 2\zeta\omega_o s + \omega_o^2} \tag{1.3}$$

and $G(s) = K < 1$. Then

$$VCO(s) = \frac{G(s)}{1 - G(s)F(s)} = K\frac{s^2 + 2\zeta\omega_o s + \omega_o^2}{s^2 + 2\zeta_1\omega_o s + \omega_o^2} \tag{1.4}$$

where $\zeta_1 = (1 - K)\zeta$. The lowering of the damping ratio is called "Q amplification" ($Q = 1/2\zeta$) and moves the poles even closer to the $j\omega$ axis. The frequency is controlled by altering the capacitance of the resonator by using a varactor diode as a capacitor. A simple circuit diagram for a resonant circuit VCO is shown in Figure 1.4, where the frequency is controlled by adjusting the reverse bias of the varactor diode C_1 [1]. Other forms of VCOs, such as crystal

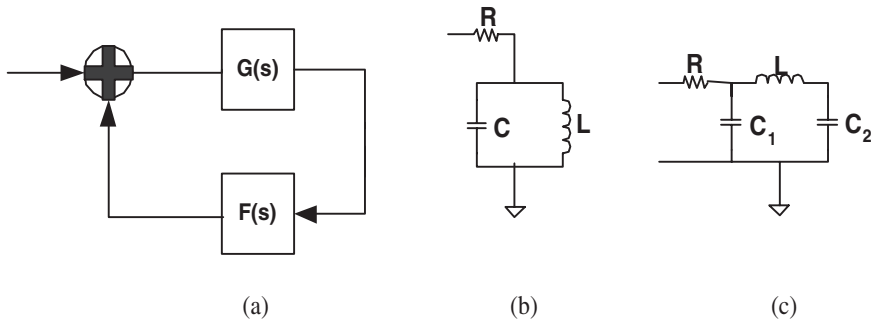


Figure 1.3: (a) Block Diagram of an Oscillator implemented as a positive feedback loop between a Voltage to current amplifier through a resonant circuit. (b) Resonant LC Tank (c) Resonant p network.

oscillators and YIG oscillators essentially run on the same principle, but modify the resonant circuit [1, 3, 4]. For the all digital and software PLLs, the VCO is replaced by a digitally or numerically controlled oscillator (DCO/NCO). In this case, the input voltage is replaced by some digital value, and the output is a digital oscillating waveform [5, 7].

The Loop Filter

As noted earlier, there is conceptually always a loop filter. Typical analysis ignores the high frequency low pass filter and other dynamics that do not affect the behaviour of the loop at the time constants of the phase. Since PLLs are mostly second order and as the VCO is modelled as an integrator, loop filters are of the lead lag type. More specifically, the loop filter contains an integrator which is able to track a phase ramp, and this corresponds to tracking a step in frequency [4, 7].

For a double integrator system, the loop filter needs a minimum phase zero to obtain stability. This is true whether the filter is implemented as an analogue or digital filter. Higher order loops can be obtained by adding extra pole/zero pairs to the filter [2]. The analogue circuits in Figure 1.5 show typical implementations active and passive loop filters [1]. The transfer function of the active section shown in Figure 1.5-b filter is fairly general and given by:

$$\frac{V_o}{V_a - V_b} = \frac{sR_2(C_2 + C_3) + 1}{sR_1C_2(sR_2C_3 + 1)} \tag{1.5}$$

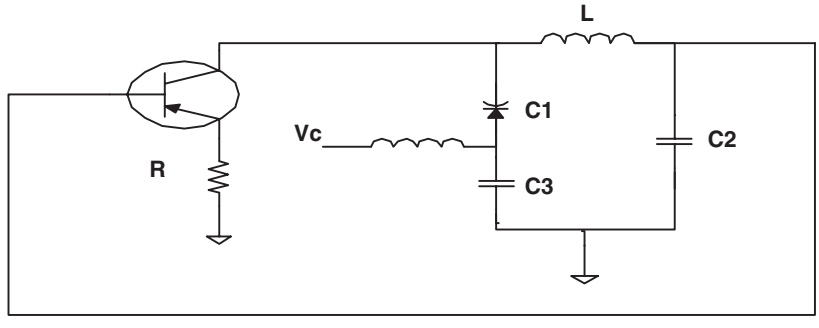


Figure 1.4: A VCO implemented through a PI network.

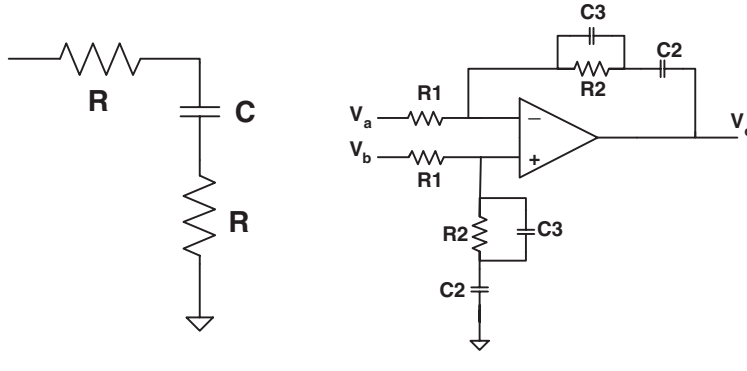


Figure 1.5: Typical Analogue Filter Sections (a) Passive Lead Lag (b) Active Lead Lag.

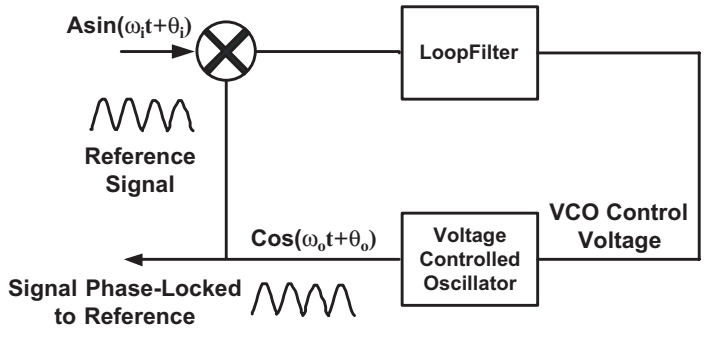


Figure 1.6: Classical Mixing PLL.

1.3.3 PLL analysis

Figure 1.6 shows the classical mixing PLL, which is mostly used to describe and analyze the PLL theoretically. However, practical loops usually resemble Figure 1.7, in which a differential amplifier, acting as a high frequency low pass filter, is used to attenuate the double frequency term and a bandpass filter is used to limit the bandwidth of input signals to the loop.

A general sinusoidal signal at the reference input of a PLL as shown in Figure 1.7 can be written as:

$$v_i = A\sin(\omega_i t + \theta_i) \tag{1.6}$$

The output signal from the Voltage Controlled Oscillator (VCO) into the mixer is given by

$$v_o = \mathrm{VCO}_{\mathrm{out}}(t) = \cos(\omega_o t + \theta_o) \tag{1.7}$$

The output of the mixer in Figure 1.7 is then given by

$$v_d = \mathrm{Mixer}_{\mathrm{out}}(t) = AK_m \sin(\omega_i t + \theta_i)\cos(\omega_o t + \theta_o) \tag{1.8}$$

where K_m is the gain of the mixer. Typically, analysis of such a PLL is done by taking several simplifying steps. Using the familiar trigonometric identity in terms of the PLL

$$2\sin(\omega_i t + \theta_i)\cos(\omega_o t + \theta_o) \tag{1.9}$$

$$\sin[(\omega_i + \omega_o)t + \theta_i + \theta_o] + \sin[(\omega_i - \omega_o)t + \theta_i - \theta_o] \tag{1.10}$$

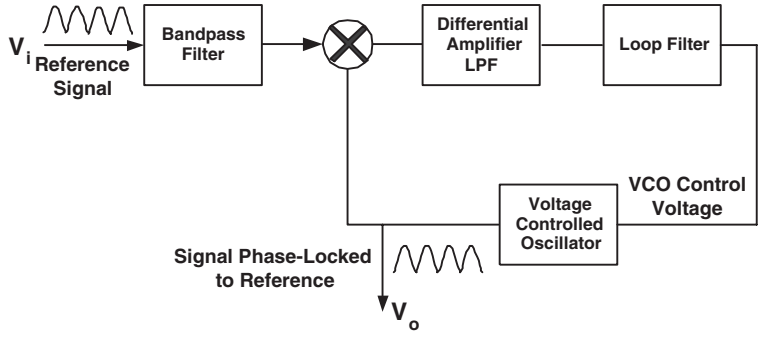


Figure 1.7: Practical PLL block diagram.

and then making the two fundamental assumptions below will lead to the commonly used model of the analogue PLL. Let $\theta_d = \theta_i - \theta_o$. Then these assumptions are

1. The first term in (1.9) is attenuated by the high frequency low pass filter in Figure 1.7 and by the low pass nature of the PLL itself.

2. $\omega_i \approx \omega_o$, so that the difference can be incorporated into θ_d. This means that the VCO can be modelled as an integrator.

The problem is that this is still a nonlinear system, and as such is in general difficult to analyze. The typical methods of analysis include:

1) *Linearization*: For θ_d small and slowly varying we have

$$\sin(\theta_d) \approx \theta_d, \quad \cos\theta_d \approx 1, \ \text{ and } \ \theta_d^2 \approx 0.$$

While this is useful for studying loops that are near lock, it does not help for analyzing the loop when θ_d is large.

2) *Phase plane portraits*: This method is a classical graphical method of analyzing the behaviour of low order nonlinear systems about a singular point. The disadvantage is that phase plane portraits can only completely describe first and second order systems.

The linearized model is shown in Figure 1.8. This is what is used for most analysis methods and measurements of PLLs. Changing the phase detector and

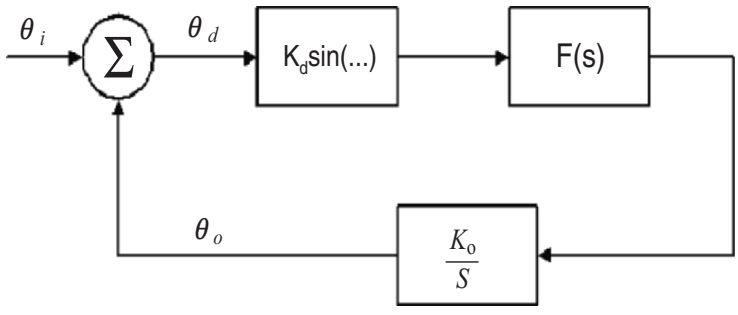


Figure 1.8: Linearized Model of the PLL.

VCO can result in a system for which this model is very accurate. Although this linear model contains useful information about the phase behaviour of the PLL, it has some very important omissions that show up in the simulating or constructing the classical PLL ,and these are [1, 5]:

1) As seen in (1.8), the amplitude of the phase error is dependent upon A, the input signal amplitude. The linearized model has a loop gain that is dependent upon the loop components. Thus, in practical loop design, the input amplitude must either be regulated or its effects on the loop must be anticipated.

2) The equations of a PLL are stiff, that is, the loop has a component at baseband and one at $2\omega_o$. The simulations of that sample fast enough to characterize the latter are often far too slow (due to the huge number of sample points) to effectively characterize the former.

The PLL model in Figure 1.8 is a closed-loop feedback system. The complimentary sensitivity transfer function from reference phase input to VCO phase output, $T(s)$, can be obtained as

$$T(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_d K_v F(s)}{s + K_d K_v F(s)} \tag{1.11}$$

Similarly, the sensitivity transfer function from the reference phase input to the phase error, $S(s)$, is

$$S(s) = \frac{\theta_d(s)}{\theta_i(s)} = \frac{s}{s + K_d K_v F(s)} \tag{1.12}$$

Among the basic properties of interest in this transfer function are the order and stability of the loop. The order of the PLL system is determined by the order of the denominator of (1.10). The stability of the system can be determined by a variety of methods including root locus, Bode plots, Nyquist plots, and Nichols charts [1].

The Hold Range

The hold range, $\Delta\omega_H$, is defined as the frequency range over which the PLL is able to statically maintain phase tracking. It is determined by calculating the frequency offset at the reference input that causes the phase error to be beyond the range of linear analysis.

Since loops will be permanently out of lock if the frequency offset at the input is greater than the hold range, this quantity has negligible effect practically, and it can be calculated for a classical PLL (sinusoidal phase detector) as [5, 11]:

$$\Delta\omega_H = K_o K_d F(0). \tag{1.13}$$

The Lock Range

The lock range, $\Delta\omega_L$, is defined as the frequency range within which the PLL locks within one single-beat note between the reference frequency and output frequency [1]. The lock range must be calculated from a nonlinear equation, but there are several useful approximations that are made. In particular, if the relative order of numerator and denominator of the PLL are 1, then the loop can be said to behave like a first order loop at higher frequencies, and thus the lock range can be estimated as [11]:

$$\Delta\omega_L \approx \pm K_o K_d F(\infty) \tag{1.14}$$

1.4 Conclusions

In this chapter we have presented a general review of phase lock loops (PLL) that included the importance of synchronization in communication, control and measurement applications. The basic components of an analog PLL were described and a complete linear analysis of the loop was given. The main parameters that describe the loop performance were also given.

Chapter 2

Digital Phase Lock Loops

2.1 Introduction

The analog PLLs (APLLs) are still widely used, but digital PLLs (DPLLs) are attracting more attention for the significant advantages of digital systems over their analog counterparts. These advantages include superiority in performance, speed, reliability, and reduction in size and cost. DPLLs alleviated many problems associated with APLLs. The following is a brief comparison:

1. APLLs suffer from the sensitivity of the voltage-controlled oscillator (which decides the center frequency) to temperature and power supply variations, hence the need for initial calibration and periodic adjustments. DPLLs do not suffer from such a problem [12, 17, 68].

2. The most familiar error detectors used in APLLs utilize analog multipliers (balanced modulators) which are sensitive to d.c. drifts [10, 18], a problem that does not exist in DPLLs.

3. DPLLs can operate at very low frequencies that create problems in APLLs [17, 18]. These problems are related to the operation of the analog low-pass filter in extracting the lower frequency component [11, 18],as it needs larger time for better frequency resolution, and this will reduce the locking speed.

4. Self-acquisition of APLLs is often slow and unreliable, while DPLLs, a basic block diagram is shown in Figure 2.1, have faster locking speeds [17]. This is due to the basic operation of the analog low-pass filter and the analog multiplier in the phase detector (PD).

The low pass filter cannot extract the lower frequency within few input cycles since the narrow time windowing will destroy the information in the frequency domain (due to the time frequency resolution tradeoff). Same reasoning applies for the balanced modulator in the PD.

In contrast, a digital filter operation is based on a difference equation with convergence decided by the coefficients of the equation, and the PD operation

is related to the instant of sampling rather than to frequency comparison. This is why a DPLL can achieve locking within few cycles (see Chapter 3).

Hence DPLLs are tackled with concentration on sinusoidal DPLLs. The development of DPLLs started in the 1970's. The analysis of the positive-going zero-crossing sinusoidal DPLL was presented in 1980 using fixed point theorems [50, 51]. The second significant step in sinusoidal DPLLs was the digital tan-lock loop (DTL) in 1982 [13] that is based on the arctan phase detector which gave linear system equation. Since 1982 many efforts were made to improve the performance of DTL [52, 53, 54, 59]. In this book we emphasize a new DPLL that combines the two major approaches in the field: the approach of sinusoidal DPLL with fixed point analysis and the approach of DTL with the arctan phase detector. The main advantages of this DPLL, called the time delay digital tan-lock loop (TDTL), is the reduced complexity of the loop, wider lock range of the first-order loop and faster convergence speed under certain choice of the TDTL parameters.

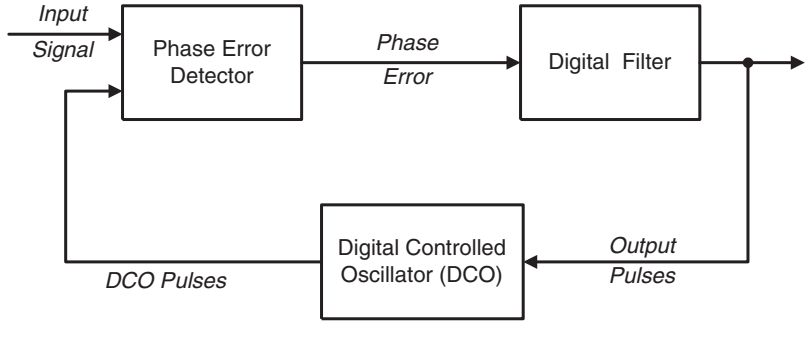


Figure 2.1: Basic block diagram of the digital phase locked loop.

2.2 Classification of DPLLs

Digital phase-locked loops can be classified into two major categories depending on the type of sampling process [12]

1. Uniform sampling DPLLs
2. Non-uniform sampling DPLLs

The DPLLs can be also classified according to the mechanization of the phase detector into five types as follows [12]

1. The flip-flop DPLL (FF-DPLL)

2. The Nyquist-rate DPLL (NR-DPLL)

3. The lead-lag DPLL (LL-DPLL), a.k.a binary-quantized DPLL (BQ-DPLL)

4. Exclusive-OR DPLL (XOR-DPLL)

5. Zero-crossing DPLL (ZC-DPLL)

Types 2 above belongs to uniform sampling, while the others belong to non-uniform sampling. A brief discussion of each type is given below.

Flip-flop DPLL

This kind of DPLLs was proposed in the literature by a number of authors [19], [20], [21] and [22].

In this type the phase detector is realized by a set-clear flip-flop and a counter as shown in Figure 2.2.

The sinusoidal input signal is converted into a square wave through an operational amplifier acting as a comparator. The output "Q" of the flip-flop is set to logic "1" on the positive-going edge of the comparator, and to logic "0" on the positive-going edge of the digital controlled oscillator (DCO). Hence the duration when Q is at level "1" will be proportional to phase error between the input signal and the DCO. This error is used to gate the counter clock which has a frequency of $2^M f_o$ where f_o is the center frequency of the DPLL and 2^M is the number of quantization levels of the phase error over period of 2π. The counter is zeroed and starts counting on the positive-going edge of the flip-flop waveform. The content of the counter, N_o, which is proportional to the phase error, is applied to the N-bit first-order digital filter which consists of proportional and accumulation paths. The output of the digital filter K controls the period of the DCO which consists basically of a programmable divide-by-K counter. It is the phase of the input signal that undergoes non-uniform sampling here rather than the amplitude.

Nyquist-rate DPLL

This DPLL was proposed in [23, 24] and subsequently developed by the works in [25], [26] and [27]. Nyquist sampling on the phase of the input signal rather than the amplitude was reported in [28]. In this DPLL the sinusoidal input signal is sampled *uniformly* at the Nyquist rate f_s and converted to N-bit digital signal by an analog-to-digital converter (ADC), then it is multiplied digitally by the DCO output $v(k)$ to form an error signal. This error signal is applied to

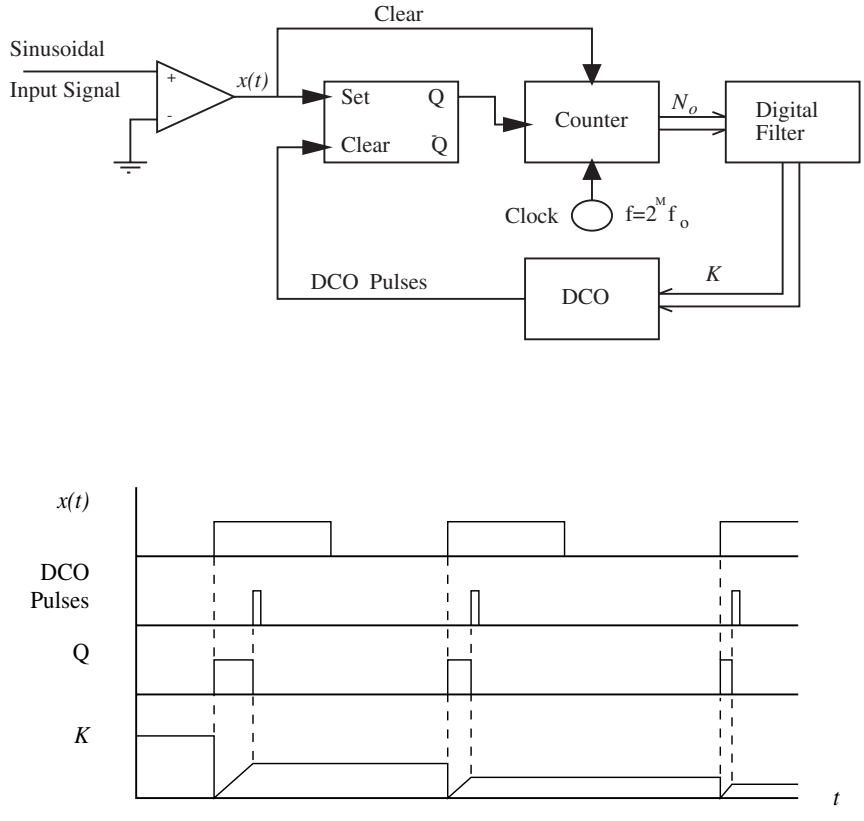


Figure 2.2: The flip-flop DPLL. Above: A block diagram. Below: Waveforms as a function of time.

N-bit digital filter whose output controls the period of the DCO as shown in Figure 2.3.

The DCO used in NR-DPLL is of algorithmic type [26]. It is constructed by utilizing the basic idea of the analog VCO. The analog VCO output can be given as in [29]

$$\mathrm{v}(t) = B\cos\left\{\omega_o t + G_o\int_{-\infty}^{t} y(\tau)d\tau\right\} \tag{2.1}$$

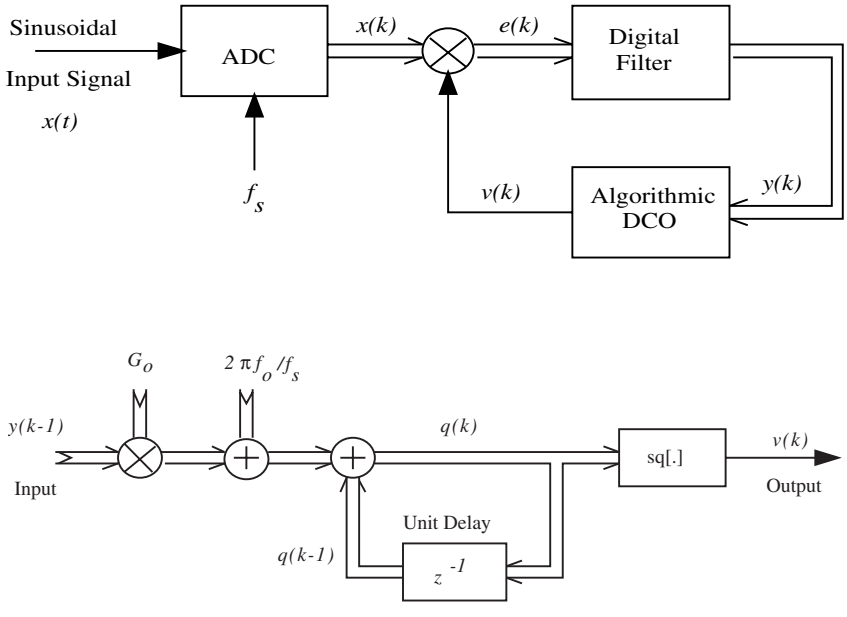


Figure 2.3: The Nyquist-rate DPLL. Above: A block diagram. Below: The algorithmic DCO.

where

$$\begin{aligned} \omega_o &= \text{center frequency of the VCO} \\ G_o &= \text{sensitivity of the VCO (rad/sec.volt)} \\ y(t) &= \text{input voltage} \end{aligned}$$

In the discrete time domain, (2.1) can be expressed as follows

$$\mathrm{v}(kT_s) = B\cos\left\{2\pi k f_o/f_s + G_o\sum_{n=0}^{k-1} y(n)\right\} \tag{2.2}$$

where $T_s = 1/f_s$ is the sampling period and $y(n) = y(nT_s)$. The sinusoidal function $\mathrm{v}(kT_s)$ is converted to a square wave $v(k)$ as follows

$$v(k) = \mathrm{sq}\left\{2\pi k f_o/f_s + G_o\sum_{n=0}^{k-1} y(n)\right\} \tag{2.3}$$

where

$$\begin{aligned} \mathrm{sq}(x) &= 1 \quad 0 \le x < \pi \\ &= -1 \quad \pi \le x < 2\pi \\ \mathrm{sq}(x) &= \mathrm{sq}(x + 2\pi) \end{aligned}$$

The direct implementation of (2.2) above is rather difficult due to the time-varying term $2\pi k f_o/f_s$. However, (2.2) can be written in the following form

$$v(k) = \mathrm{sq}\left[\sum_{n=0}^{k-1}\{2\pi k f_o/f_s + y(n)\}\right] = \mathrm{sq}[q(k)] \tag{2.4}$$

where

$$q(k) = \sum_{n=0}^{k-1}\{2\pi k f_o/f_s + y(n)\} \tag{2.5}$$

It can be shown that

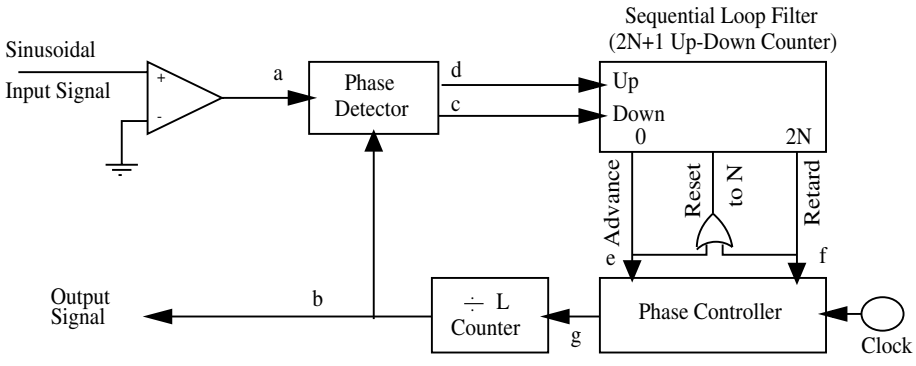
$$q(k) = q(k-1) + 2\pi f_o/f_s + G_o y(k-1) \tag{2.6}$$

Figure 2.3 shows the algorithmic DCO block diagram based on (2.3).

Lead-Lag DPLL

This type of DPLLs has been developed by the work in [30, 31] and extended in [32] to include a second-order sequential filter with memory. The LL-DPLL is characterized by the binary output of the phase detector that indicates whether the DCO waveform leads or lags the input signal. Due to this quantization it is often named "binary quantized DPLL". The input sinusoidal signal should be converted to a square wave by a comparator.

On the occurrence of a DCO pulse, either "lead" or "lag" terminal of the phase detector will give a pulse depending on the state of the input signal being "high" or "low", respectively, as shown in Figure 2.4. These pulses are applied to a special type of digital filters known as "sequential filter." The sequential filter deals with the input "lead" and "lag" pulses statistically; it observes them for a variable duration of time and gives a decision when a reliable limit is reached. Figure 2.4 shows that the sequential filter is composed of an up-down counter whose length is $2N + 1$. A pulse at the "lead" terminal causes the content of the counter to increase by 1, while the "lag" pulse behaves conversely. When the content of the counter reaches $2N$ or zero, the corresponding "Retard" (or: "Advance") output gives a pulse that resets the counter to "N" and triggers the phase controller. A "Retard" pulse causes the phase controller to delete one pulse



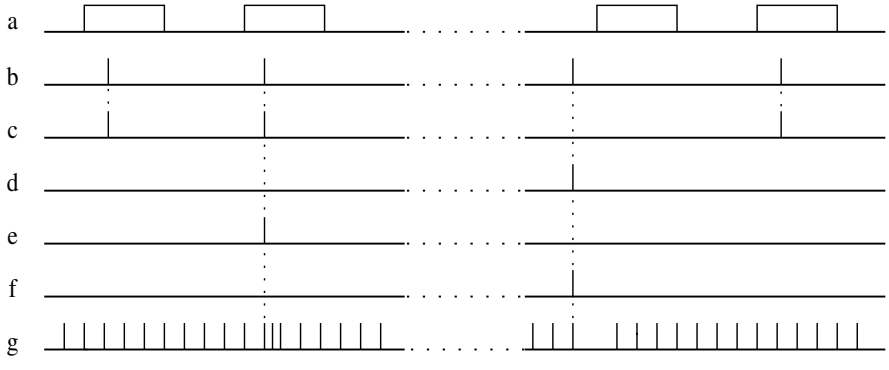


Figure 2.4: The lead-lag DPLL with associated waveforms.

from the clock pulse train that is applied to the divide-by-L counter, forcing the DCO phase to retard by $2\pi/L$, where L is the number of quantization levels of the period 2π. An "Advance pulse does the contrary.

When "lead" and "lag" pulses are equally probable, a case that indicates locking, the counter cycle has maximum duration. Other types of sequential filters exist like the N-before-M filter [12] and the variable reset random walk filter [32].

Exclusive-OR DPLL

Greer has utilized an exclusive-OR gate as a phase detector [17]. He used a K-counter as a digital filter and an increment-decrement (I/D) counter with a divide-by-N counter as a DCO. Figure 2.5 shows a block diagram of the Exclusive-OR DPLL.

The phase error detector (PED) compares the phase of the input signal, ϕ_{in}, with that of the loop output, ϕ_{out}, and gives an error signal ϕ_d defined as follows

$$\phi_d = K_o \, \phi_e \tag{2.7}$$

where K_o is the gain of the PED and $\phi_e = \phi_{in} - \phi_{out}$. The output of the PED can also be expressed as follows

$$\phi_d = (\%H - \%L)/100(\text{cycles}) \tag{2.8}$$

where $\%H$ and $\%L$ represent percentage "high" and "low" logic levels, respectively, during one cycle. Hence ϕ_d (in cycles) varies between +1 and -1. When $\phi_e = 1/4$ cycle ($\pi/2$ rad) then $\%H = \%L$ as shown in Figure 2.5-b, hence $\phi_d = 0 \equiv 2\pi \pmod{2\pi} = 1$ cycle, therefore $K_o = 4$.

The output of the phase detector controls the operation of the K-counter which consists of two divide-by-K counters, an up-counter and a down-counter, both triggered by a clock of rate Mf_o, where f_o is the center frequency and M is an integer. The output "C" of this counter, which is connected to the increment input (INR) of the I/D counter, generates a pulse when the K-counter ends an "up" cycle, while the "borrow" output B which is connected to the decrement input (DCR) generates a pulse on the end of a "down" cycle. A pulse applied to the "INR" input adds 1/2 cycle to the I/D output, while a pulse on the "DCR" input deletes 1/2 cycle.

The I/D counter clock runs at a frequency of $2Nf_o$, where N is the modulus of the divide-by-N counter that follows the I/D counter. The I/D counter is merely a divide-by-2 counter if no "INR" or "DCR" pulses are applied, hence its output frequency can be given by

$$\begin{aligned} F &= Nf_o + 1/2[K_o\phi_e M f_o/K] \ \text{(Hz)} \\ &= Nf_o + 2\phi_e M f_o/K \end{aligned} \tag{2.9}$$

The factor 1/2 above came from the fact that the I/D counter adds or deletes half a cycle when "INR" or "DCR" pulses are applied, respectively.

The output frequency can be expressed as

$$f_{out} = f_o + 2\phi_e M f_o/(KN) \quad \text{(Hz)} \tag{2.10}$$

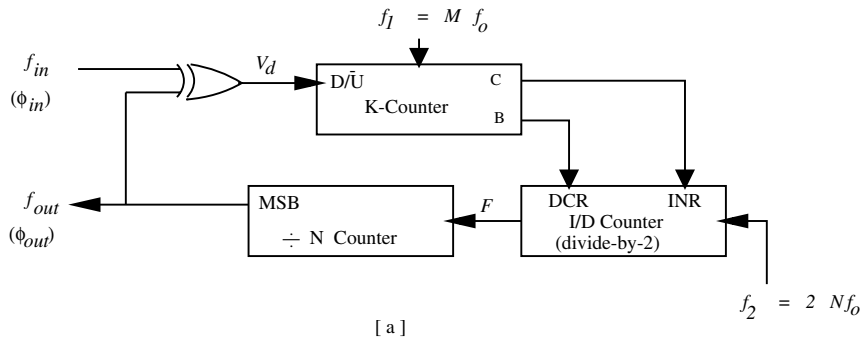
Since ϕ_d varies between $+1$ and -1, ϕ_e varies between $+1/4$ and $-1/4$ cycles, hence lock range can be derived as follows

$$\begin{aligned} \Delta &= |f_{in} - f_o|_{\max} \\ &= |f_{out} - f_o|_{\max} \\ &= Mf_o/(2KN) \\ \text{lock range} &= 2\Delta = Mf_o/(KN) \end{aligned} \tag{2.11}$$

There exists a phase error between the input and the output signals even at locking, i.e. when $f_{out} = f_{in}$, which is given by [17]

$$\phi_e = KN(f_{in} - f_o)/(2Mf_o) \tag{2.12}$$

Figure 2.5-d clarifies this relationship.



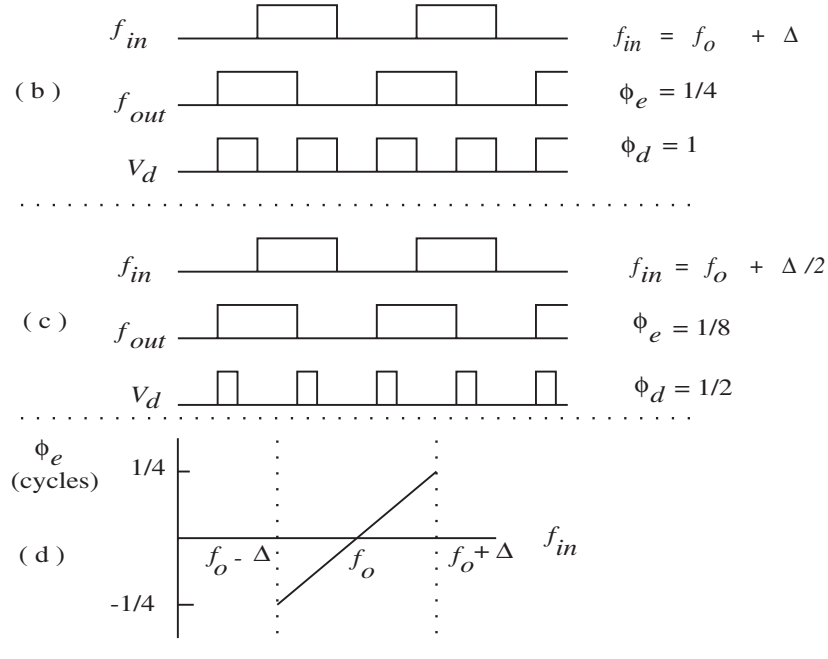


Figure 2.5: The Exclusive-OR DPLL with associated waveforms. (a) Block diagram. (b) Waveforms at $f_{in} = f_o + \Delta$. (c) Waveforms at $f_{in} = f_o + \Delta/2$. (d) Transfer function at lock.

Zero-Crossing DPLL

This type of DPLLs accepts sinusoidal signals and samples the input signal at or near zero crossings, hence the name zero-crossing DPLL (ZC-DPLL).

There are two variations of ZC-DPLLs. The first, named $ZC_1 - DPLL$, samples only on the positive-going zero crossings, while the other type, $ZC_2 - DPLL$, samples on both positive and negative-going zero crossings. The first type is the most important type of DPLLs since it is the simplest to implement, the easiest to model, and its operation and performance are indicative of the general behavior of any DPLL [12]. Although $ZC_2 - DPLL$ locks faster, it has additional design complications over $ZC_1 - DPLL$ [12, 111], hence the latter dominated.

$ZC_2 - DPLL$ has been proposed first in [33] and developed later as discussed in [34] and [35]. $ZC_1 - DPLL$ has been developed by the work in [36, 37, 38, 39, 40, 41, 42]. The systematic statistical analysis of $ZC_1 - DPLL$ is provided in [43] where it presents a numerical solution to the Chapman-Kolmogorov equation. Other studies on this have also been presented in the literature [44, 45, 46, 47, 48, 49, 50, 51]. In 1982 a new classification was imposed on DPLLs by the advent of the digital tanlock loop (DTL) [13]. $ZC_1 - DPLL$ and $ZC_2 - DPLL$ were given the name "sinusoidal ZC-DPLL" or simply "sinusoidal DPLL" [13], based on the phase detection technique. DTL is a new type of $ZC_1 - DPLLs$ that has distinguished phase detection mechanism and significant advantages over other types of DPLLs. Many efforts have been made to improve the characteristics of DTL and its application in communication systems [52, 53, 59].

A brief description of the sinusoidal $ZC_1 - DPLL$ and DTL is given below.

Sinusoidal $ZC_1 - DPLL$

Figure 2.6 shows the block diagram of sinusoidal $ZC_1 - DPLL$ with the associated waveforms. Here the function of phase detection is merged with that of non-uniform sampling since the instant of sampling determines the phase error [38, 50]. The main parts of this DPLL are explained below.

The N-bit Digital Filter

This filter modifies the analog-to-digital converter (ADC) samples, which are applied to the DCO, in such a way that leads the phase error to reach a constant value and hence locking occurs. The digital filter consists of proportional and accumulation paths.

The order of the digital filter represents the order of its difference equation, hence the n^{th}-order digital filter can be described in the z-domain by the

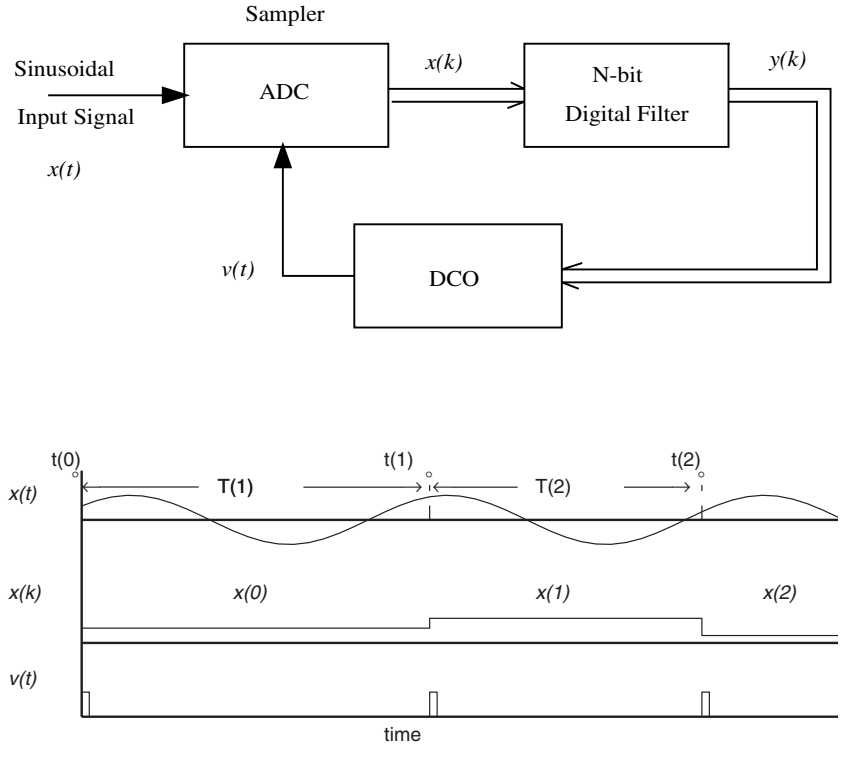


Figure 2.6: The Sinusoidal $ZC_1 - DPLL$ with associated waveforms.

following transfer function [39]

$$D(z) = \kappa \frac{(z+c_1)(z+c_2)...(z+c_n)}{(z+p_1)(z+p_2)...(z+p_n)} \tag{2.13}$$

Since the present value of the phase error depends on the previous value, the order of the loop equals the order of the digital filter plus one. Hence in the first-order loop the digital filter is just a proportional path, while the second-order loop utilizes a first-order digital filter with the following transfer function

$$D(z) = \kappa(z+c_1)/(z+p_1) \tag{2.14}$$

For the second-order sinusoidal $ZC_1 - DPLL$ to lock on zero phase error, p_1 must equal -1 [39], hence (2.14) may be written in a more convenient form as follows

$$D(z) = G_1 + G_2/(1 - z^{-1}) \tag{2.15}$$

which gives in the time domain the following input-output relation

$$y(n) = G_1\, x(n) + G_2 \sum_{k=0}^{n} x(k) \tag{2.16}$$

where $x(k)$ and $y(k)$ are the discrete input and output signals, respectively.

The Digital Controlled Oscillator (DCO)

The digital controlled oscillator consists of a programmable counter, a binary subtracter, and zero detector. Figure 2.7 shows a block diagram of DCO with associated waveforms. Subtraction is performed using a 2's complementer and a full adder. The counter content is decremented by one on the occurrence of each clock pulse. When it reaches zero, the counter generates a pulse at the output. This pulse is used to load the counter with the binary number $M - K$ where M is a constant number and K is the input number. The number M decides the DCO free-running frequency f_o when the input number K is zero as follows

$$f_o = f_c/M \tag{2.17}$$

where f_c is the frequency of the counter clock. The period between the $(k-1)^{th}$ and the k^{th} pulses is given by

$$T(k) = (M - K)\, T_c \tag{2.18}$$

where $T_c = 1/f_c$.

The Phase Equation

The input signal $x(t)$ is assumed to be in the form

$$x(t) = A\ \sin\{\omega_o t + \theta(t)\} + n(t) \tag{2.19}$$

where A is the signal amplitude, $\omega_o = 2\pi f_o$, $\theta(t)$ is the information bearing phase, and $n(t)$ is Gaussian additive noise. For a frequency step input $\theta(t)$ is given by

$$\theta(t) = (\omega - \omega_o)t + \theta_o \tag{2.20}$$

where θ_o is a phase constant and ω is the input frequency. Under such condition the (nonlinear) difference equations representing the first-order loop (with

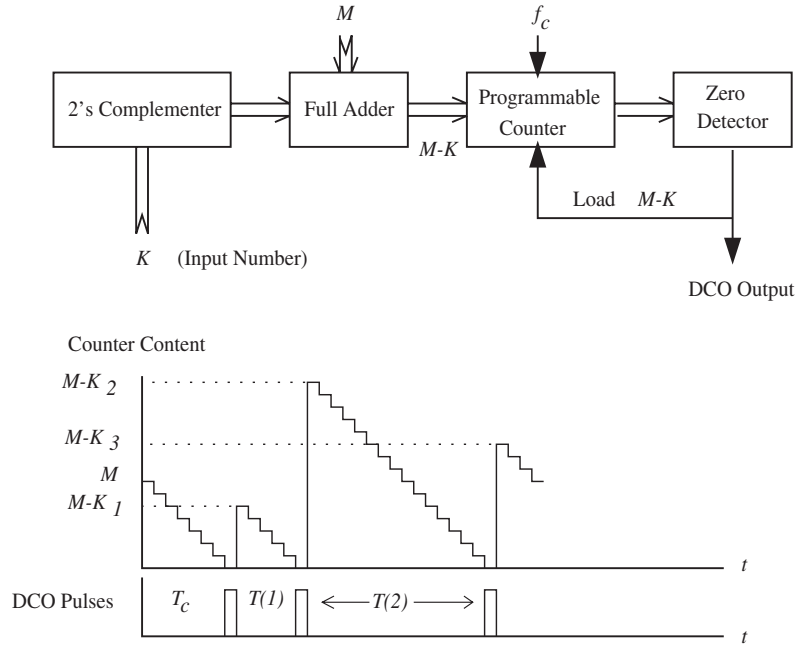


Figure 2.7: The digital controlled oscillator with associated waveforms.

$D(z) = G_1$) and the second-order loop (with $D(z) = G_1 + G_2 z/(z-1)$) can be respectively given by [50, 51]

$$\phi(k+1) = \phi(k) - K_1^{'} \sin\{\phi(k)\} - K_2^{'} n(k) + \Lambda_o \tag{2.21}$$

and

$$\begin{aligned} \phi(k+1) &= 2\phi(k) - \phi(k-1) + K_1^{'} \sin\{\phi(k)\} \\ &\quad -K_2^{'} n(k) - r[K_1^{'} \sin\{\phi(k)\} + K_2^{'} n(k)] \end{aligned} \tag{2.22}$$

where $\phi(k)$ is the phase error at the instant k, $K_1^{'} = \omega G1\ A$, $K_2 = \omega G_1$, $\Lambda_o = 2\pi(\omega - \omega_o)/\omega_o$, and $r = 1 + G_2/G_1$. From these equations it can be shown that the noise-free steady-state phase error of the first-order loop is given by

$$\phi_{ss} = \sin^{-1}(\Lambda_o / K_1^{'}) \tag{2.23}$$

while the second-order loop locks on zero phase error.

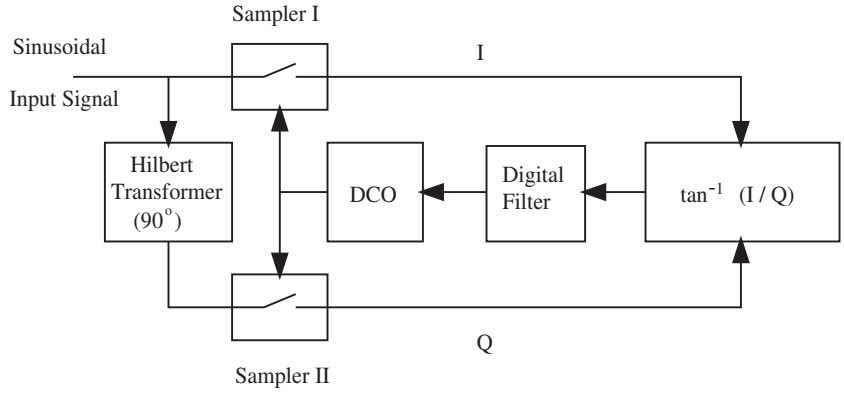


Figure 2.8: Structure of the digital tanlock loop.

Although sinusoidal DPLL has many advantages over other types of DPLLs [12], it has the shortcomings of sensitivity to the variations in the input signal power and rather limited lock range. The DTL explained below has solved these problems.

The Digital Tanlock Loop (DTL)

This DPLL was introduced in [13]. Figure 2.8 shows a block diagram of DTL. It is composed of 90^o phase shifter, two samplers, a phase error detector, a digital loop filter, and a digital controlled oscillator (DCO). Sampler I takes a sample I of the incoming signal, and sampler II takes a sample Q of the phase-shifted version of the incoming signal simultaneously. The phase error, which is determined by the sampling instant, is extracted by the $\tan^{-1}$ function at the phase error detector. This phase error is modified by the digital filter whose output controls the period of the digital controlled oscillator (DCO). This technique in the phase detection along with the use of a Hilbert transformer led to a linear phase difference equation.

The noise-free difference equations of the first and second-order DTLs are given respectively by [13]

$$\phi(k+1) = (1 - K_1^{'})\phi(k) + \Lambda_o \tag{2.24}$$

and

$$\phi(k+2) = (2 - rK_1^{'})\phi(k+1) + (K_1^{'} - 1)\phi(k) \tag{2.25}$$

where all symbols are defined in the paragraph of sinusoidal $\mathrm{ZC}_1 - \mathrm{DPLL}$.

The steady-state phase error of the first-order DTL is

$$\phi_{ss} = \Lambda_o / K_1^{'} \tag{2.26}$$

and the second-order DTL locks on zero phase error. Due to dividing the input signal by its phase-shifted version at the phase error detector, DTL noise-free performance is independent of the signal amplitude A, hence under noise-free condition DTL is insensitive to the variations in signal power. The first-order DTL has wider lock range than the sinusoidal DPLL.

The analysis of sinusoidal DPLL is nonlinear and based on "fixed point theorems" [50, 51], while the analysis of the DTL is linear. Our work in this book combines the two major approaches in the field: the approach of sinusoidal DPLL built on fixed point analysis and the approach of tanlock based on the arctan phase detection. Our main objective is to reduce the complicated structure of DTL while preserving its advantages.

2.3 Conclusions

In this chapter we have presented a survey of digital phase-locked loops (DPLLs). The survey included the major classification of DPLLs according to the sampling scheme where they are classified as uniform and non-uniform sampling DPLLs. Further classification according to the phase detection scheme was also considered. The main parts in each class are clarified.

It has been shown that the most important kind of DPLLs is the non-uniform sampling sinusoidal zero-crossing DPLL (ZC-DPLL). Hence we will concentrate on this kind of DPLLs in this book. Developments in this respect are presented. Two major approaches exist in this field: the original approach of sinusoidal DPLL built on fixed point analysis and the approach of tanlock phase detection. In this book we will present a combination of the above two approaches that will give many advantages over the existing types of DPLLs.

Chapter 3

The Time-Delay Digital Tanlock Loops (TDTLs)

3.1 Introduction

Phase-locked loops play an important role in communication systems since they contribute significantly to a variety of applications like filtering, frequency synthesis, frequency modulation, demodulation, signal detection, motor-speed control and many other applications [11]. Digital phase-locked loops (DPLLs) were introduced to alleviate some of the problems associated with the analog loops like sensitivity to d.c. drifts and the need for initial calibration and periodic adjustments. Nonuniform sampling DPLLs are the most important digital phase-locked loops because they are simple to implement and easy to model [12]. Digital tanlock loop (DTL), proposed in [13], has introduced several significant advantages over other nonuniform sampling digital phase locked loops. It allows a wider locking range of the first-order loop and a reduced sensitivity of the locking conditions to the variation of the input signal power [13]. DTL proved to be efficient for many applications in digital communications (see, for example, [53, 54]). The constant 90^o phase-shifter is a vital part of this conventional DTL (CDTL) and all of its modifications (see, for instance, [56, 57]). In fact, a digital Hilbert transformer introduces approximations and imposes limitations on the range of input frequencies, especially when implemented on a microprocessor [60, 61].

In this chapter, a constant time-delay unit is used to produce a phase-shifted version of the incoming signal. This method reduces the complexity of the phase-shifter and avoids the limitations and other problems that accompany the 90^o phase-shifter.

Except for the linearity of the characteristic function of the phase error detector, the main advantages of CDTL are maintained by TDTL despite its

reduced structure. First, under noise-free conditions its performance is not affected by the variation of signal power. Second, the first-order loop can have wider lock range than other sinusoidal DPLLs (including CDTL) if the circuit parameters are properly chosen. The region of locking independently of initial phase errors in the first-order loop can be made larger than that of the first-order CDTL since the conditions of independent locking are less stringent in TDTL as a result of non-linearity.

Although the lock range of the second-order TDTL is reduced as compared to that of CDTL, this reduction is not a severe short-coming since it mainly concerns high values of the loop gain K_1 which are not desired [13]. In fact, any range of input frequencies can be handled after a suitable arrangement of the circuit parameters.

In the following section, a general description of TDTL is given. In Section 3.3, the system is analyzed and locking conditions are derived for the first- and second-order TDTLs.

3.2 Structure and System Equation

3.2.1 Structure of the TDTL

The structure of TDTL is similar to that of CDTL in Figure 2.8 except for the technique of phase-shifting. A block diagram of TDTL is shown in Figure 3.1. It is composed of a time-delay unit (τ), two samplers, a phase error detector, a digital loop filter, and a digital controlled oscillator (digital clock). Sampler I takes a sample $x(k)$ of the time-delayed version of the incoming signal, and sampler II takes a sample $y(k)$ of the incoming signal simultaneously. The phase detector takes the function $\mathrm{Tan}^{-1}[x(k)/y(k)]$ at every sampling instant, where Tan^{-1} is the four-quadrant arctan function. The output of the phase error detector, $e(k)$, is a function of the phase error between the incoming signal and the digital clock at the k^{th} sampling instant in modulo (2π) sense. The digital filter is used to modify the output of the phase error detector $e(k)$ and provide a control signal to the digital clock to decide the next sampling instant at the two samplers. Hence the sampling is nonuniform, and the loop arranges its frequency at the digital clock to be, in the limit, equal to the input frequency with a minimum phase difference.

3.2.2 System Equation

Under noise-free conditions, the loop accepts a sinusoidal input signal $y(t)$ having a radian frequency ω with a frequency offset $\Delta\omega(=\omega-\omega_o)$ from the nominal

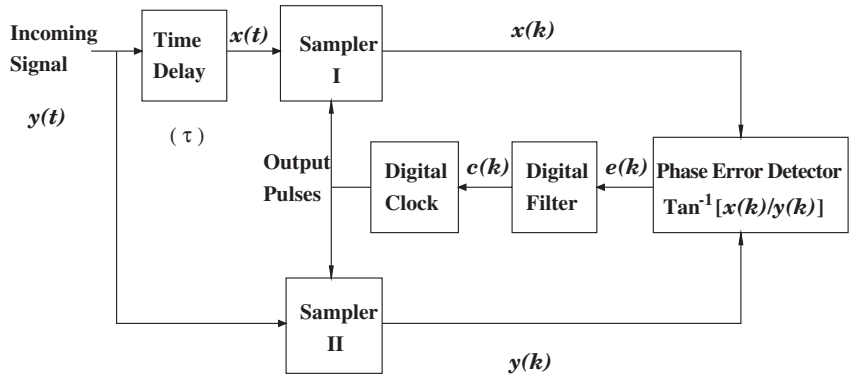


Figure 3.1: Block diagram of the time-delay digital tanlock loop.

radian frequency ω_o of the digital clock. The input signal is given by

$$y(t) = A \sin[\omega_o t + \theta(t)] \tag{3.1}$$

where A is the signal amplitude and $\theta(\mathrm{t})=\Delta\omega\mathrm{t}+\theta_o$ is the phase process of the incoming signal, θ_o being a constant. The signal is assumed not to have a d.c. component. The time-delay unit introduces a constant time-delay τ in the input signal which causes a phase lag $\psi(=\omega\tau)$ proportional to input radian frequency ω. It is worth noting that in the CDTL of Figure 2.8, the phase lag is frequency-independent $\psi = \pi/2\ \forall\omega$. Hence, the following analysis can contain the CDTL as a special case.

The time-delayed version of the TDTL input signal, denoted by $x(t)$, can be expressed as

$$x(t) = A \sin[\omega_o t + \theta(t) - \psi] \tag{3.2}$$

At the k^{th} sampling instant, the sampled values of $y(t)$ and $x(t)$ are given respectively by

$$y(k) = A \sin[\omega_o t(k) + \theta(k)] \tag{3.3}$$

and

$$x(k) = A \sin[\omega_o t(k) + \theta(k) - \psi] \tag{3.4}$$

where $\theta(k) = \theta[t(k)]$.

The sampling interval between the sampling instants $t(k)$ and $t(k-1)$ is given by

$$T(k) = \mathcal{T}_o - c(k-1) \tag{3.5}$$

where $\mathcal{T}_o(=\frac{2\pi}{\omega_o})$ is the nominal period of the digital clock and $c(i)$ is the output of the digital filter at the i^{th} sampling instant. Assuming $t(0) = 0$, the total time $t(k)$ up to the k^{th} sampling instant is

$$t(k) = \sum_{i=1}^{k} T(i) = k\mathcal{T}_o - \sum_{i=0}^{k-1} c(i) \tag{3.6}$$

Thus, $y(k)$ and $x(k)$ can be written as

$$y(k) = A\sin[\theta(k) - \omega_o \sum_{i=0}^{k-1} c(i)] \tag{3.7}$$

and

$$x(k) = A\sin[\theta(k) - \omega_o \sum_{i=0}^{k-1} c(i) - \psi] \tag{3.8}$$

The phase error $\phi(k)$ is defined as

$$\phi(k) = \theta(k) - \omega_o \sum_{i=0}^{k-1} c(i) - \psi \tag{3.9}$$

Now $y(k)$ and $x(k)$ can be expressed as

$$y(k) = A\sin[\phi(k) + \psi] \tag{3.10}$$

and

$$x(k) = A\sin[\phi(k)] \tag{3.11}$$

From equations (3.6) and (3.9) it can be shown that

$$\phi(k+1) = \phi(k) - \omega c(k) + \Lambda_o \tag{3.12}$$

where $\Lambda_o = 2\pi\frac{\omega-\omega_o}{\omega_o}$. This is the system equation of TDTL; it is similar to that of CDTL. Note that if $D(z)$ is the transfer function of the digital filter, then $c(k) = h_D(k) * e(k)$, where $h_D(k) \overset{Z.T.}{\longleftrightarrow} D(z)$ and $e(k)$ is the output of the phase error detector at the k^{th} sampling instant.

3.2.3 The Characteristic Function

If we define $f[\alpha] = -\pi + \{(\alpha + \pi) \text{ modulo } (2\pi)\}$, then $e(k)$ is given by

$$e(k) = f\left[\text{Tan}^{-1}\left(\frac{\sin\{\phi(k)\}}{\sin\{\phi(k)+\psi\}}\right)\right] \tag{3.13}$$

Thus, the characteristic function $h_\psi(\phi)$ of the phase error detector is nonlinear and depends on the input frequency ω and the time delay τ; it is given by

$$h_\psi(\phi) = f\left[\mathrm{Tan}^{-1}\left(\frac{\sin(\phi)}{\sin(\phi+\psi)}\right)\right] \tag{3.14}$$

The function $h_\psi(\phi)$ can equivalently be expressed in terms of the ratio $W\{=\frac{\omega_o}{\omega}\}$ and the nominal phase shift $\psi_o(=\omega_o\tau)$ as follows

$$h_\psi(\phi) = f\left[\mathrm{Tan}^{-1}\left(\frac{\sin(\phi)}{\sin(\phi+\frac{\psi_o}{W})}\right)\right] \tag{3.15}$$

The four-quadrant $\mathrm{Tan}^{-1}(\frac{x}{y})$ function used by the phase detector can distinguish between the four quadrants according to the signs of x and y unlike the ordinary $\tan^{-1}(.)$ function. Using this property of the phase detector it can be shown that the function $h_\psi(\phi)$ is continuous in ϕ over the interval $(-\pi,\pi)$ by taking the limits at the suspected points where $\sin(\phi+\psi)=0$, also we can prove that $\frac{dh_\psi(\phi)}{d\phi}$ is continuous over $(-\pi,\pi)$ (see Appendix). The continuity of $h_\psi(\phi)$ and its first derivative makes it possible to analyze the circuit performance using fixed point theorems [50, 51].

3.3 System Analysis

In this section the performance of the first- and second-order TDTLs is studied in the absence of noise for an input with a frequency offset. Locking conditions, locking independently of initial phase error, and steady-state phase error are considered. Comparisons with CDTL are made whenever appropriate.

3.3.1 First-order TDTL

The first-order loop utilizes a digital filter having just a positive proportionality constant G_1. Thus the system equation (3.12) becomes

$$\phi(k+1) = \phi(k) - K_1^{'}\, h_\psi[\phi(k)] + \Lambda_o \tag{3.16}$$

where $K_1^{'} = \omega G_1$. If K_1 is defined to be $\omega_o G_1$ then $K_1^{'} = K_1/W$.

A. Locking Conditions

To see whether the system represented by (3.16) will finally reach a steady-state, we follow the same analysis given by Osborne [50]. First, we seek a fixed point of the equation

$$g(\phi) = \phi - K_1^{'}\, h_\psi(\phi) + \Lambda_o \tag{3.17}$$

that is, a solution ϕ_{ss} such that

$$\phi_{ss} = g(\phi_{ss}) \tag{3.18}$$

The sequence $\{\phi(k)\}$ defined by (3.16) will converge (locally) to the solution ϕ_{ss}, i.e., $\lim_{k\to\infty}[\phi(k)] = \phi_{ss}$ if

$$|g^{'}(\phi_{ss})| < 1 \tag{3.19}$$

provided that $g(\phi)$ is continuously differentiable at the fixed point ϕ_{ss}. Knowing that $h_{\psi}(\phi)$ is continuously differentiable over $(-\pi, \pi)$, it is easy to see that $g(\phi)$ is also continuously differentiable over $(-\pi, \pi)$. Now from (3.13), (3.14), (3.17), and(3.18) it can be shown that

$$e_{ss} = f\left[\mathrm{Tan}^{-1}\left(\frac{\sin(\phi_{ss})}{\sin(\phi_{ss}+\psi)}\right)\right] = \frac{\Lambda_o}{K_1^{'}} \tag{3.20}$$

where e_{ss} is the steady-state output of the phase error detector. Since $|f\,[.]| < \pi$, we must have

$$|\Lambda_o/K_1^{'}| < \pi \tag{3.21}$$

From (3.20) it can be shown that

$$\tan(\phi_{ss}) = \frac{\sin(\psi)\tan(\eta)}{1-\cos(\psi)\tan(\eta)} \tag{3.22}$$

where $\eta = \Lambda_o/K_1^{'}$. We now postpone the task of finding the exact expression for ϕ_{ss} and define β and α by

$$\beta = \frac{\sin(\psi)\tan(\eta)}{1-\cos(\psi)\tan(\eta)} = \frac{\sin(\psi)}{\cot(\eta)-\cos(\psi)} \tag{3.23}$$

$$\alpha = \tan^{-1}(\beta) \tag{3.24}$$

where $\tan^{-1}(.)$ is the ordinary arctan over$(-\frac{\pi}{2}, \frac{\pi}{2})$. Then it follows that

$$\phi_{ss} = \alpha + j\pi\ , \quad j \in \{-1, 0, 1\} \tag{3.25}$$

From (3.14), (3.17) and (3.19) we obtain

$$|1 - \frac{K_1^{'}\sin(\psi)}{\sin^2(\phi_{ss}) + \sin^2(\phi_{ss}+\psi)}| < 1 \tag{3.26}$$

Using (3.24) we get

$$|1 - \frac{K_1^{'}\sin(\psi)}{\sin^2(\alpha) + \sin^2(\alpha+\psi)}| < 1 \tag{3.27}$$

Knowing that $K_1' = K_1/W$, $\psi = \psi_o/W$, and $\Lambda_o = 2\pi(1-W)/W$, the inequalities (3.21) and (3.27) lead to

$$2|1-W| \;<\; K_1 \;< 2W\,\frac{\sin^2(\alpha)+\sin^2(\alpha+\psi)}{\sin(\psi)}$$

or equivalently

$$2|1-W| \;<\; K_1 \;< 2W\,\frac{\sin^2(\alpha)+\sin^2(\alpha+\psi_o/W)}{\sin(\psi_o/W)} \tag{3.28}$$

Since $K_1 > 0$, we must have

$$0 \;<\; f\,[\psi] \;<\; \pi \tag{3.29}$$

The inequality (3.28) can be solved numerically to find the lock range of the first-order TDTL. Figure 3.2 shows the major range of locking for different values of ψ_o. If ψ_o increases beyond π, the lock range begins to separate. It can also be seen that under a suitable choice of ψ_o (e.g. $\psi_o = \pi$), TDTL can have wider lock range than CDTL.

B. The Region of Independent Locking

Inequality (3.28) ensures locking only in a neighborhood of ϕ_{ss} where $\phi(k)$ leads to $\phi(k+1)$ inside $(-\pi,\pi)$ such that the phase "locks" finally on ϕ_{ss}. Hence locking occurs for some range of values of the initial phase error $\phi(0)$ but not necessarily for all values. If the incoming signal has a single frequency (not modulated) within the lock range, changing the initial phase error would result in locking. But in many applications, like tracking M-ary FSK signals, the input frequency is modulated, i.e. having different values. Transition from one frequency to another gives different steady-state phase errors ϕ_{ss} according to equations (3.22-3.25). Each ϕ_{ss} would be the initial phase error $\phi(0)$ for the next incoming frequency. To track (demodulate) such signals, the loop should lock on all incoming frequencies (within the lock range) for all possible values of $\phi(0)$ in the range $(-\pi,\pi)$, i.e. independently of the initial phase error. Since independent locking entails further condition(s), the range of independent locking is always a subspace of the range of lock.

Inside the lock range of the first-order CDTL, the region in which $|\phi(k+1)|$ can exceed π is excluded entirely from the range of independent locking [13]. For TDTL this is no longer true owing to the non-linearity of the characteristic function $h(\phi)$. At some points of the lock range, the case when $|\phi(k+1)| > \pi$ may only cause some cycle slips, therefore these points cannot be excluded from the range of independent locking.

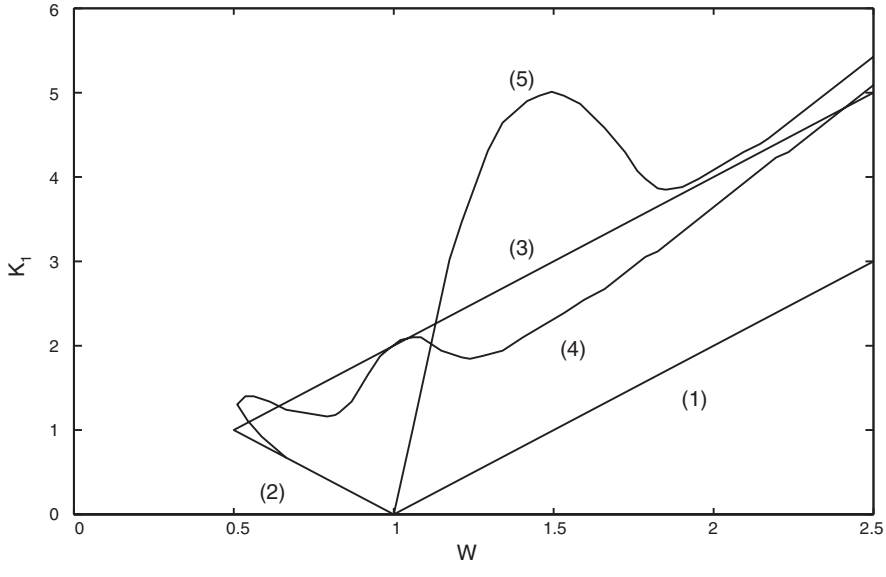


Figure 3.2: Major range of locking of the first-order TDTL for different values of $\psi_o = \omega_o \tau$. Note: the region enclosed by (1), (2), and (3) is for CDTL; the region enclosed by (1), (2) and (4) is for TDTL when ψ_o=$\pi/2$; and the region enclosed by (1) and (5) is for TDTL when $\psi_o = \pi$.

It is true, however, that if $|\phi(k+1)| < \pi$ for all $\phi(k) \in (-\pi, \pi)$ at some point of the lock range, then this point is in the range of independent locking. This is ensured if the extrema of the function y given below lie inside $(-\pi, \pi)$.

$$y = \phi - K_1^{'}\, h_\psi(\phi) + \Lambda_o,\ \phi \in (-\pi, \pi) \tag{3.30}$$

These extrema can occur at $\phi = \pm\pi$ or at the critical points of y which exist only when $|\frac{K_1^{'} \sin(\psi)-1}{\cos(\psi)}| < 1$ and can be expressed after suitable manipulations as

$$\phi_i = f\,[\frac{1}{2}\{\,\pi(i+\frac{n}{2}) - \psi + (1-2(i\ \ \mathrm{modulo}(2)))\sin^{-1}(\kappa)\}] \tag{3.31}$$

where $i \in \{0,1,2,3\}$, $\kappa = (K_1^{'}\sin(\psi) - 1)/|\cos(\psi)|$, $n = 1$ or -1 according as $f\,[\psi] < \frac{\pi}{2}$ or $f\,[\psi] > \frac{\pi}{2}$, respectively, keeping in mind that $0 < f\,[\psi] < \pi$. The case $f\,[\psi] = \frac{\pi}{2}$ is excluded here as it corresponds to conventional DTL.

Hence, if the function y above intersects the line $y_1(\phi) = \phi$ at a point $\phi = \phi^* \in (-\pi, \pi)$ such that $|y^{'}(\phi^*)| < 1$, then TDTL is inside the lock range according to (3.19), and it would lock on the input frequency with $\phi_{ss} = \phi^*$

independently of the initial phase error $\phi(0)$ if the above extrema of y lie inside $(-\pi, \pi)$. If one of these extrema exceeds the range $(-\pi, \pi)$, there are two cases to handle:
1) if y does not intersect the line $y_2(\phi) = \phi + 2\pi$ or the line $y_3(\phi) = \phi - 2\pi$, $\phi \in (-\pi, \pi)$, then locking occurs independently of initial phase error $\phi(0)$.
2) if y intersects either y_2 or y_3 at a point $\phi = \phi^{**} \in (-\pi, \pi)$, then locking occurs independently of the initial phase error only when $|y^{'}(\phi^{**})| > 1$. This leads to the following condition

$$| 1 - \frac{K_1^{'} \sin(\psi)}{\sin^2(\alpha_1) + \sin^2(\alpha_1 + \psi)} | > 1 \tag{3.32}$$

where

$$\alpha_1 = \tan^{-1} \left(\frac{\sin(\psi)\tan(\eta \pm \frac{2\pi}{K_1^{'}})}{1 - \cos(\psi)\tan(\eta \pm \frac{2\pi}{K_1^{'}})} \right)$$

If this case happens for CDTL, we have $y^{'}(\phi^{**}) = y^{'}(\phi^{*})$ due to linearity, hence $|y^{'}(\phi^{**})| < 1$ and locking would be dependent on the initial phase error.

Thus the actual range of independent locking for TDTL can be found only by a numerical search throughout the range of locking. Figure 3.3 shows this range for $\psi_o = \frac{\pi}{2}$; it is wider than that of first-order CDTL.

C. The Steady-state Phase Error ϕ_{ss}

Let the four quadrants of phase be defined as $Q_1 = [0, \frac{\pi}{2}]$, $Q_2 = (\frac{\pi}{2}, \pi)$, $Q_3 = (-\pi, -\frac{\pi}{2})$, and $Q_4 = [-\frac{\pi}{2}, 0)$, noting that $\pm\pi$ are excluded. The actual value of ϕ_{ss} can be obtained from (3.20) by careful consideration of the four quadrants. For example, let $\eta \{= \Lambda_o / K_1^{'}\} \in Q_2$ and consider all angles to be measured modulo (2π) so that $f[.]$ can be dropped off. Then we have
(i) $\sin(\phi_{ss}) > 0$, which implies $\phi_{ss} \in Q_1$ or Q_2.
(ii) $\sin(\phi_{ss} + \psi) < 0$, which implies $\phi_{ss} + \psi \in Q_3$ or Q_4

Thus, $\psi \in Q_1$ implies that $\phi_{ss} \in Q_2$ or Q_3, and $\psi \in Q_2$ implies $\phi_{ss} \in Q_1$ or Q_2 (noting that $0 < \psi < \pi$). The steady-state phase error ϕ_{ss} can now be expressed as

$$\phi_{ss} = \begin{cases} \alpha & \beta > 0 \text{ and } \psi \in Q_2 \\ -\pi + \alpha & \beta > 0 \text{ and } \psi \in Q_1 \\ \pi + \alpha & \beta < 0 \end{cases}$$

Noting that $\beta > 0$ implies $\psi \in Q_2$, ϕ_{ss} can be re-expressed as

$$\phi_{ss} = \begin{cases} \alpha & \beta > 0 \\ \pi + \alpha & \beta < 0 \end{cases}$$

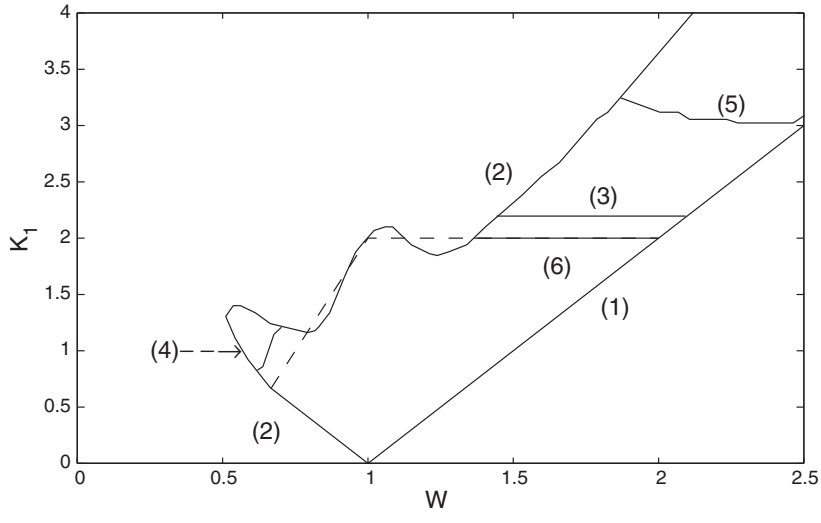


Figure 3.3: The range of independent locking of the first-order TDTL when ψ_o=$\pi/2$. Note: the region enclosed by (1), (2), and (6) and the region enclosed by (1), (3), (2), and (5) are for TDTL; the region enclosed by the tetragon is for CDTL.

Following the same reasoning as above and noting that $\beta = 0$ implies and is implied by $\eta = 0 \in Q_1$, it can be shown that

$$\phi_{ss} = \begin{cases} \alpha & \text{if } \eta \in Q_1 \text{ and } \beta \geq 0\ , \\ & \quad \eta \in Q_2 \text{ and } \beta > 0\ , \\ & \quad \eta \in Q_3 \text{ and } \beta < 0\ , \\ & \text{or } \eta \in Q_4 \text{ and } \beta > 0 \\ f\left[\alpha + \pi\right] & \text{otherwise.} \end{cases}$$

More succinctly, ϕ_{ss} can be expressed as

$$\phi_{ss} = \begin{cases} \alpha & \beta \sin(\eta) \geq 0 \\ f\left[\alpha + \pi\right] & \text{otherwise.} \end{cases} \tag{3.33}$$

For the first-order CDTL we have $\phi_{ss} = \eta = \Lambda_o / K_1^{'}$, which is dependent on $W = \omega_o/\omega$ and $K_1^{'} = K_1/W$. For the first-order TDTL, ϕ_{ss} is a function of the above parameters in addition to $\psi = \psi_o/W$, as can be seen from eqs.(3.33), (3.24) and (3.23). Hence, for the same W and K_1, the relationship between the steady-state phase errors of CDTL and TDTL is decided by $\psi_o = \omega_o \tau$.

D. Simulation Results

Example 1:

Consider a modulation-free input signal $y(t) = \sin(\omega t + \theta_o)$, θ_o = constant. Assume that the loop center frequency ω_o and the time-delay τ are arranged such that $\psi_o = \omega_o \tau = \pi/3$, and that G_1 is chosen such that $K_1 = G_1 \omega_o = 1.4$. Note that the specific choice of ω_o is application dependent and not important in this analysis since only the ratio $W = \omega_o/\omega$ and the product $\omega_o \tau$ are considered. Once chosen, ω_o and τ are constant.

Now let the incoming frequency be such that $W = 0.9$ (i.e. the incoming frequency ω is more than the loop center frequency ω_o). This value is inside the lock range since it satisfies (3.28). It is also inside the range of independent locking since all of the extrema of y, (3.30), lie inside $(-\pi, \pi)$. Figure 3.4 shows the locking phase process of TDTL for initial phase error $\phi(0) = \theta_o - \psi = -1$ (rad). The phase plane is plotted modulo (2π). Figure 3.4 also shows the sampling process of TDTL on the delayed version of the input signal, $x(t)$, as in (3.11). TDTL arranges its frequency to be equal to the input frequency ω in few steps. The steady-state phase error is $\phi_{ss} = 0.5001$ (rad), in accordance with (3.33). To study the convergence (locking) speed, we define the relative error between the input frequency ω and TDTL output frequency at the k^{th} sampling interval as

$$E(k) = \frac{|\omega - \frac{2\pi}{T(k)}|}{\omega}$$

and the convergence indicator k_c as

$$k_c = k \text{ at which } E(k+n) < \epsilon \text{ for } n = 0, 1, 2, ...$$

where ϵ is a small positive number. This indicator decides the locking (convergence) speed and is important in dealing with modulated signals. In this example $\epsilon = 0.01$ is considered and we have $k_c = 3$, i.e. locking occurs approximately at the third sampling instant. For CDTL with same parameters K_1, W and $\phi(0)$ as above we have $k_c = 7$. The same ratio between the convergence indicators of TDTL and CDTL is approximately true for all values of the initial phase error $\phi(0)$ in this example. Therefore, the convergence speed is nearly doubled in this case by using TDTL with $\psi_o = \pi/3$. Further studies on convergence behavior would be presented later in this chapter.

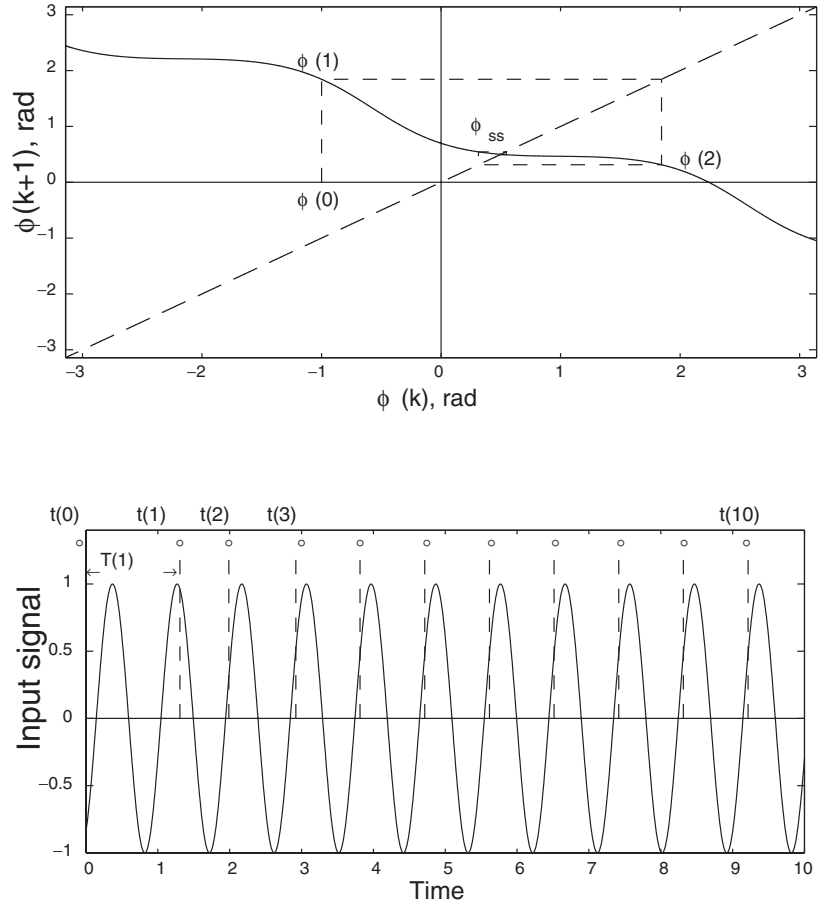


Figure 3.4: Above: Locking phase process of the first-order TDTL for $\psi_o = \omega_o\tau = \pi/3$, $K_1 = 1.4$, $W = 0.9$ and $\phi(0) = -1$ (rad), plotted modulo (2π). Locking occurs independently of the initial phase error $\phi(0)$. Below: Sampling process of TDTL on the delayed version of the input signal, $x(t)$, for the above parameters.

Example 2:

Now we consider a binary FSK input signal with two frequencies ω_1 and ω_2 such that $W_1 = \omega_o/\omega_1 = 0.8$ and $W_2 = \omega_o/\omega_2 = 1.1$. Assume $\psi_o = \omega_o\tau = \pi/2$ and $K_1 = G_1\omega_o = 1$. According to Figure 3.2, the loop can lock on both frequencies independently of the initial phase errors. The minimum value of the input frequencies, which is decided by f_o and the range of independent locking, should be reasonably larger than the symbol rate R to ensure locking.

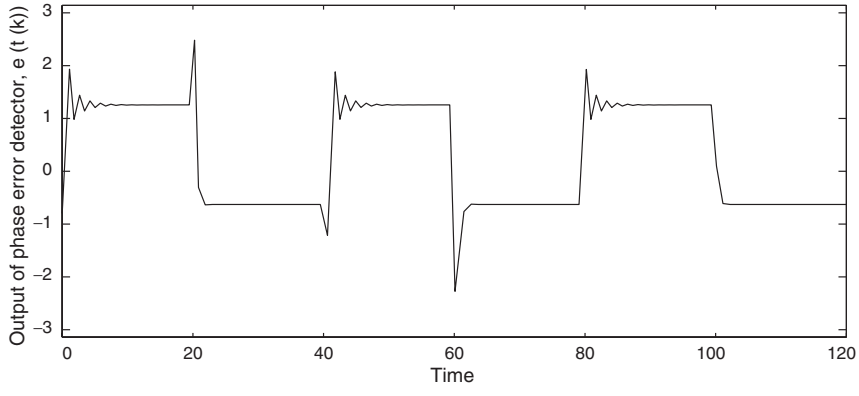


Figure 3.5: Tracking a binary FSK signal using the first-order TDTL with $W_1 = \omega_o/\omega_1 = 0.8$, $W_2 = \omega_o/\omega_2 = 1.1$, $\psi_o = \omega_o\tau = \pi/2$ and $K_1 = G_1\omega_o = 1$.

A loop with higher convergence speed can handle higher R for a fixed f_o. For clarity we take in this example $f_o/R = 20$. Figure 3.5 shows the output of the phase error detector, $e(k)$, as a function of time for this signal. The two values of e_{ss} are 1.2566 (rad) and -0.6283 (rad), in accordance with (3.20).

3.3.2 Second-Order TDTL

The second-order TDTL utilizes a proportional-plus accumulation digital filter with a transfer function $D(z)$ given by

$$D(z) = G_1 + G_2/(1 - z^{-1}) \tag{3.34}$$

where G_1 and G_2 are positive constants. From eqs.(3.34) and (3.12), the system equation of the second-order TDTL can be obtained as

$$\phi(k+2) = 2\phi(k+1) - \phi(k) - rK_1^{'}e(k+1) + K_1^{'}e(k) \tag{3.35}$$

where $r = 1 + G_2/G_1$ and $K_1^{'} = G_1\omega$.

A. Locking Conditions

In the steady-state we have $\phi(k+2) = \phi(k+1) = \phi(k)$, hence $e(k+1) = e(k)$. Therefore, the steady-state value of the output of the phase detector e_{ss} is zero. From (3.13) it is evident that the steady-state phase error ϕ_{ss} is $n\pi$ (n being an integer). Since $f[\phi_{ss}] \neq \pm\pi$ we must have $f[\phi_{ss}] = 0$, hence $\phi_{ss} = 2m\pi$ (m being an integer).

Following the same fixed point analysis as that given by Osborne [51], the locking conditions can be obtained from the condition that the *eigenvalues* of the matrix G given by

$$G = \begin{bmatrix} 0 & 1 \\ -1 + K_1^{'} \csc(\psi) & 2 - rK_1^{'} \csc(\psi) \end{bmatrix}$$

must be less than 1. If $0 < f[\psi] < \pi$, then the matrix G is similar to that given in [51], (2.9), with $K_1^{'}$ replaced by $K_1^{'}\csc(\psi)$. Thus, we have the following conditions

$$0 < K_1 < \frac{4}{1+r} W \sin\left(\frac{\psi_o}{W}\right), \; r > 1 \tag{3.36}$$

If $-\pi < f[\psi] < 0$, G will be similar to the matrix in (2.11) obtained [51] with $K_1^{'}$ replaced by $-K_1^{'}\csc(\psi)$ and conditions that are mutually exclusive with (3.35) are obtained. Therefore, we will consider $f[\psi]$ to be in the interval $(0, \pi)$ only, adding the following condition

$$0 < f[\psi] < \pi \tag{3.37}$$

Figure 3.6 shows the major range of locking of the second-order TDTL for different values of ψ_o. Although the lock range is reduced in comparison to the lock range of the second-order CDTL, any range of input frequencies can be handled after suitable modification of the circuit parameters, keeping in mind that high values of K_1 in the lock range of CDTL are not desired [13].

B. The Region of Independent Locking

As for the range of locking independently of initial phase errors $\phi(0)$ and $\phi(1)$, numerical search throughout the lock range has showed that the range of independent locking is still bounded by the conditions of independent locking for the second-order CDTL given by

$$\frac{2W}{r+1} \; < \; K_1 \; < \; \frac{4W}{r+1} \tag{3.38}$$

and

$$0 \; < \; K_1 \; < \; \frac{2W}{r-1} \tag{3.39}$$

These conditions can also be obtained from (3.35) by assuming that $|\phi(k+2)| < \pi$ when $|\phi(k+1)| = |\phi(k)| = \pi$, and noting that

$$\lim_{\phi \to \pi^-} h_\psi(\phi) = \pi, \quad \lim_{\phi \to -\pi^+} h_\psi(\phi) = -\pi,$$

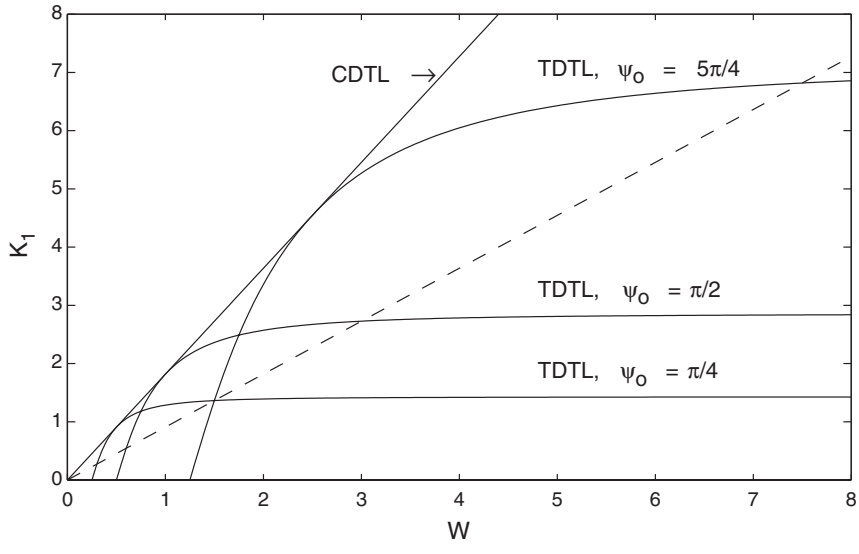


Figure 3.6: Major range of locking of the second-order CDTL and TDTL for different values of ψ_o ($r = 1.2$). Note: lock range is the area under the suitable curve. The ranges of independent locking for CDTL and TDTLs are the areas enclosed by the dashed line and the appropriate curves.

and that the other limits, $\lim_{\phi \to \pi^+} h_\psi(\phi)$ and $\lim_{\phi \to -\pi^-} h_\psi(\phi)$, are not considered as they are outside the interval $(-\pi, \pi)$. It is worth noting that the above two conditions are independent of ψ_o.

Figure 3.6 shows the boundaries of independent locking with $r = 1.2$ for the second-order CDTL and TDTL with different values of ψ_o.

3.4 Locking Speed

In this section, the convergence behavior of the TDTL in the absence of noise is analyzed. This analysis concentrates on the actual number of steps necessary for convergence of the phase error to within a radius ϵ of the steady-state phase error. In [50] and [52], the convergence behavior of the first-order sinusoidal DPLL and CDTL are analyzed based on Lipschitz constant. We adopt the similar approach here, using different values of the circuit parameters.

3.4.1 Convergence of the First-Order TDTL

The first-order TDTL utilizes a digital filter with a positive proportionality constant G_1 only. The system equation is given by (3.16) as follows:

$$\phi(k+1) = \phi(k) - K_1^{'} h_\psi[\phi(k)] + \Lambda_o$$

where $K_1^{'} = \omega G_1$, $K_1 = \omega_o G_1$, and $K_1^{'} = K_1/W$.

The locking range of the first-order TDTL is shown in Figure 3.2 for different values of ψ_o. In the analysis below, it should be noted that the choice of the loop parameters ω_o and τ will decide the lock range as in Figure 3.2, where $\psi_o = \omega_o \tau$, while the choice of the parameter K_1 and the frequency ratio $W = \omega_o/\omega$ should ensure that the loop is inside the lock range. The steady-state phase error at the input of the phase error detector was derived as [70].

$$\phi_{ss} = \begin{cases} \alpha & \beta \ \sin(\lambda) \geq 0 \\ f\,[\alpha + \pi] & \text{otherwise,} \end{cases} \tag{3.40}$$

where

$$\begin{aligned} \lambda &= \Lambda_o / K_1^{'} \\ \beta &= \frac{\sin(\psi)}{\cot(\lambda) - \cos(\psi)} \\ \alpha &= \tan^{-1}(\beta). \end{aligned} \tag{3.41}$$

The characteristic function $h_\psi(\phi)$ and its first derivative are continuously differentiable in the principal interval $(-\pi, \pi)$, hence fixed point analysis is applicable to the TDTL [70]. Following fixed point analysis developed in [50] for the sinusoidal digital phase-locked loop, the Lipschitz constant for the first-order TDTL can be given by

$$L = \max \left| \frac{g(\phi) - g(\phi_{ss})}{\phi - \phi_{ss}} \right| \tag{3.42}$$

where $g(\phi) = \phi - K_1^{'} h_\psi(\phi) + \Lambda_o$. The asymptotic estimate (upper bound) to the number of steps required for convergence of the phase error $\phi(k)$ within a radius ϵ of the fixed point ϕ_{ss} is given by [50]

$$m = \text{int} \left[\frac{\ln(\epsilon / |\phi - \phi_{ss}|)}{\ln(L)} \right] + 1 \tag{3.43}$$

where int[.] is the integer function.

It can be shown that the time required to reach the fixed point ϕ_{ss} is given by

$$T_c = m T_o W + (\phi(m) - \theta_o + \psi)/\omega \approx m T_o W \tag{3.44}$$

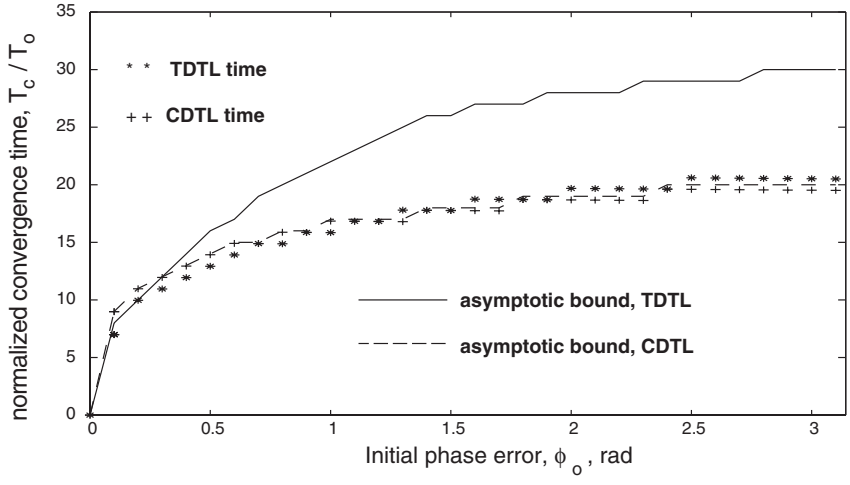


Figure 3.7: Normalized convergence time with asymptotic bounds for the first-order TDTL ($\psi_o = \pi/3$) and CDTL with phase step input ($W = 1$), $\epsilon = 0.01$, and $K_1 = 0.25$.

where $(\phi(m) - \theta_o + \psi) \lll \omega$. This is the same as CDTL case, with Lipschitz bound $m = |1 - K_1'|$ [52].

Numerical simulation showed that, unlike the case of CDTL, Lipschitz bound m is not a tight limit for M, the true number of steps for convergence. This is true for all values of TDTL parameters. The difference $m - M$ increases with the absolute difference of the initial phase ϕ_o from the steady-state phase error ϕ_{ss}.

Figure 3.7 shows the normalized convergence time, T_c/T_o, based on simulation, along with the asymptotic normalized convergence time based on Lipschitz constant as given by (3.44), for a phase step input (i.e. $W = 1$), $\psi_o = \pi/3$, and $K_1 = 0.25$. For a phase step input we have $\phi_{ss} = 0$, as in (3.40). Although the asymptotic convergence time for TDTL is higher than the actual convergence time, the actual convergence time is essentially the same as that of CDTL for all values of K_1 and ψ_o.

Figure 3.8 shows the normalized convergence time with the asymptotic bound for a frequency step input $W = 0.9$ (i.e. the input frequency, ω, is higher than the nominal loop frequency, ω_o), $K_1 = 0.25$, and $\psi_o = \pi/3$. Note that for both CDTL and TDTL, the loop converges instantly at $\phi_o = \phi_{ss}$. Although the asymptotic convergence time for TDTL is higher than that of CDTL, the actual convergence time is much less. Hence, for a robust estimation of the convergence time of TDTL, a numerical study is essential. This is rather similar to the discrepancy found in [50] for the sinusoidal DPLL. Note that the characteristic

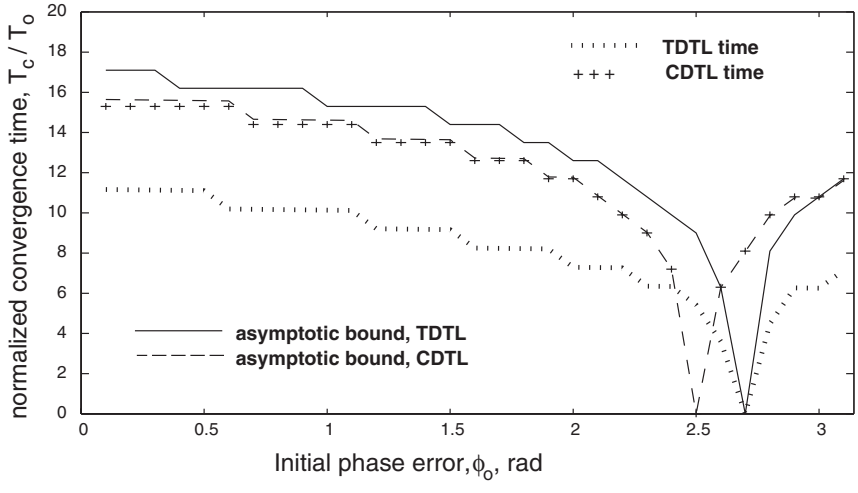


Figure 3.8: Normalized convergence time with asymptotic bounds for the first-order TDTL ($\psi_o = \pi/3$) and CDTL with frequency step input ($W = 0.9$), $\epsilon = 0.01$, and $K_1 = 0.25$.

function of the phase error detector is non-linear for TDTL and the sinusoidal DPLL, while it is linear for CDTL.

In Figure 3.9, the normalized convergence times for CDTL and TDTL for the same parameters as above and different values of TDTL nominal phase shift ψ_o. The value of ψ_o is decided by the center frequency ω_o and the time-delay τ. Hence, by a suitable arrangement of the parameters ω_o, K_1, and τ, the locking speed of TDTL can be made higher than that of CDTL.

3.5 Conclusions

A nonuniform-sampling time-delay digital tanlock loop (TDTL) has been presented, where the conventional constant 90^o phase-shifter is replaced by a time-delay unit. This is to avoid many of the practical problems associated with the implementation of the digital Hilbert transformer which is an essential part of CDTL and all of its modifications. These problems include approximations, frequency limitations, and implementation complexity. Although non-linearity is introduced in the analysis of the loop, the most important merits of CDTL over other sinusoidal DPLLs are preserved. The first-order TDTL has wider lock range, wider range of independent locking, and faster convergence than CDTL if the circuit parameters are properly chosen.

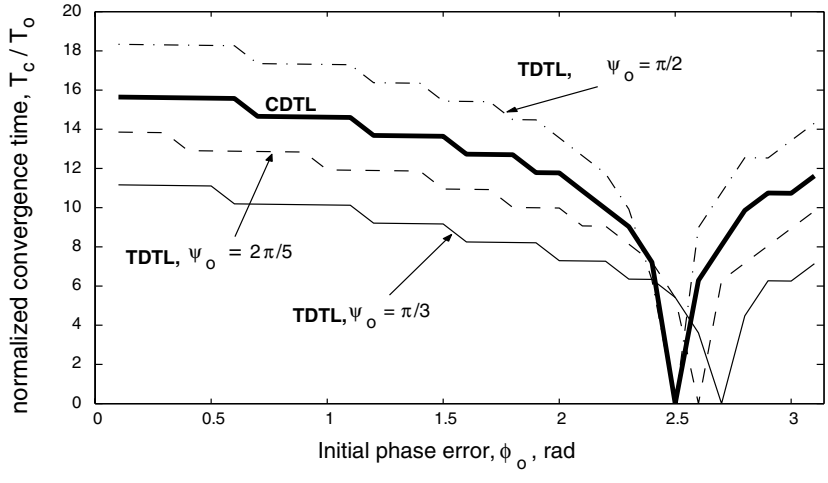


Figure 3.9: Normalized convergence time for the first-order TDTL (different values of ψ_o) and CDTL with frequency step input ($W = 0.9$), $\epsilon = 0.01$, and $K_1 = 0.25$.

We discussed the convergence behavior of the first-order TDTL. It is found that, unlike the conventional digital tanlock loop (CDTL), the asymptotic bound of the number of steps required for convergence based on Lipschitz constant diverges from the actual number of steps. This difference increases with the absolute difference of the initial phase from the steady-state phase error. For both CDTL and TDTL, convergence speed decreases as the initial phase error diverges from the steady-state phase error. Numerical study showed that the first-order TDTL locks as fast as CDTL for a phase step input for all ranges of the effective parameters, although the Lipschitz asymptotic bound for TDTL is higher than that of CDTL in this case. For a frequency step input, the first-order TDTL locks faster than CDTL under suitable arrangement of the loop parameters: the time-delay τ, the center frequency ω_o, and the loop gain K_1.

Appendix

The characteristic function $h_\psi(\phi)$, defined by (3.14), is continuous in ϕ over the interval $(-\pi, \pi)$. This can be seen by considering the limits when ϕ approaches the suspected points at which $\sin(\phi + \psi) = 0$. Consider $0 < \psi < \pi$, which is the basic version of the locking condition $0 < f[\psi] < \pi$ (see Section 3.3). Now in the interval $(-\pi, \pi)$, $\sin(\phi + \psi) = 0$ implies $\phi + \psi = 0$ or π. Consider the point at which $\phi + \psi = \pi$. Hence $0 < \phi < \pi$ and $\sin(\phi) > 0$. Then the left and

right limits of the characteristic function are equal at this point as follows

$$\begin{aligned}\lim_{\phi+\psi\to\pi^-} f\left[\mathrm{Tan}^{-1}\frac{\sin(\phi)}{\sin(\phi+\psi)}\right] &= \lim_{\phi+\psi\to\pi^-} f\left[\mathrm{Tan}^{-1}\frac{\sin(\phi)}{0^+}\right] \\ &= \lim_{\phi+\psi\to\pi^-} f\left[\frac{\pi}{2}\right] = \frac{\pi}{2}\end{aligned}$$

and

$$\begin{aligned}\lim_{\phi+\psi\to\pi^+} f\left[\mathrm{Tan}^{-1}\frac{\sin(\phi)}{\sin(\phi+\psi)}\right] &= \lim_{\phi+\psi\to\pi^-} f\left[\mathrm{Tan}^{-1}\frac{\sin(\phi)}{0^-}\right] \\ &= \lim_{\phi+\psi\to\pi^-} f\left[-\frac{3\pi}{2}\right] = \frac{\pi}{2}\end{aligned}$$

The point at which $\phi+\psi=0$ can be handled similarly.

Since α and $f[\alpha]=-\pi+\{(\alpha+\pi)\text{modulo }(2\pi)\}$ differ only by a constant, their derivatives are the same. Hence we have after some manipulations

$$\frac{dh_\psi(\phi)}{d\phi}=\frac{\sin(\psi)}{\sin^2(\phi)+\sin^2(\phi+\psi)}$$

It is clear that for $0<f[\psi]<\pi$, which is a locking condition for both first and second-order TDTLs (Section 3.3), the denominator of $\frac{dh_\psi(\phi)}{d\phi}$ is always positive, hence $\frac{dh_\psi(\phi)}{d\phi}$ is continuous in ϕ over the interval $(-\pi,\pi)$.

Chapter 4

Hilbert Transformer and Time-Delay

4.1 Introduction

Hilbert Transform (HT) is a significant tool in mathematics, physics, and signal analysis wherever Fourier techniques are used to represent or analyze functions or signals.

In the continuous-time domain the Hilbert transform $\mathbf{s}(t)$ of the function $s(t)$ is given by the following linear operation [61]

$$\begin{aligned} \mathbf{s}(t) &= \mathcal{H}[s(t)] = \frac{1}{\pi}\mathrm{P}\Big[\int_{-\infty}^{\infty} \frac{s(r)}{t-r}\, dr\Big] \\ &= \lim_{\substack{L\to\infty \\ \delta\to 0}} \frac{1}{\pi}\Big[\int_{-L}^{t-\delta} \frac{s(r)}{t-r}\, dr \;+\; \int_{t+\delta}^{L} \frac{s(r)}{t-r}\, dr\Big] \end{aligned} \tag{4.1}$$

where the Cauchy principal value (P) is used here to ensure convergence of the integral. It is apparent that $\mathcal{H}[s(t)]$ represents the convolution of $s(t)$ with $1/\pi t$.

If the signal is causal, the real and the imaginary parts of its Fourier transform are related by Hilbert transform integral, a fact of importance in signal analysis [62].

Hilbert transformers are widely used in modulation theory [61, 63]. The statistical properties of a signal $s(t)$ in noise can be obtained in a more succinct fashion by utilizing Hilbert Transform representation of the signal and the concept of the analytic signal $z(t)$ associated with $s(t)$ which is defined as [63, 64]

$$z(t) = s(t) + j\ \mathcal{H}[s(t)] \tag{4.2}$$

In time-frequency signal analysis, which is a powerful tool to deal with non-stationary signals, the discretization of the time-frequency distribution (TFD)

of any signal $s(t)$ creates aliasing problem that reduces the acceptable signal frequency range to $\omega_{\max} \leq \omega_s/4$ instead of the Nyquist bound $\omega_{\max} \leq \omega_s/2$ in the continuous-time analysis [64] ($\omega_{\max}$ being the highest frequency in the signal and ω_s the sampling radian frequency). However, the introduction of the analytic signal (defined above) eliminates the aliasing problem by eliminating the negative frequencies from the spectrum of the signal $s(t)$, which results in significant enlargement of the frequency range and clearer study of the signal [64, 65].

The transfer function $H(jw)$ of the system represented by (4.1) is given in continuous-time by [61]

$$H(j\omega) = \begin{cases} -j & \omega \geq 0 \\ 0 & \omega = 0 \\ j & \omega < 0 \end{cases} \tag{4.3}$$

and in discrete-time by [62]

$$H(e^{j\omega}) = \begin{cases} -j & 0 \leq \omega < \pi \\ 0 & \omega = 0 \\ j & -\pi \leq \omega < 0 \end{cases} \tag{4.4}$$

The above transfer functions, in continuous-time or discrete-time, represent a -90^o phase-shift operation on the input signal $s(t)$ in the frequency range $0 \leq \omega < \infty$ in the continuous time and $0 \leq \omega < \pi$ in the discrete-time. The output signal is a delayed version of the input signal and therefore HT is considered in this general sense as a time-delay phase-shifting system. The difference is that HT produces a signal-dependent delay and signal-independent phase-shift, while the time-delay system gives a signal-independent delay and signal dependent phase-shift. Hence in some signal processing systems it may be possible to replace a HT by a time-delay. If this is possible, significant reduction in the system complexity can be achieved since the time-delay is much easier to implement than the complicated Hilbert transformer [61, 62]. Recently this idea has been proposed in the area of digital phase-locked loops [70, 71] (see also Chapter 2) in an attempt to reduce the complexity of the signal processing system and to avoid the limitations and other problems that accompany the implementation of the HT [61, 60]. This resulted in similar performance of the new system except that non-linearity was introduced in the system equation. In addition, locking speed can be doubled and locking range of the first-order loop can be extended by suitable arrangement of the time-delay with other circuit parameters, a fact that is not verified by the signal-independent system using Hilbert transformer. This idea may be applied to other areas in signal processing.

The behavior of the HT in additive Gaussian noise was considered in [13] in a context of digital phase-locked loops (DPLLs). In this chapter we concentrate on the behavior of the time-delay τ as a phase-shifter for sinusoidal signals in the presence of Gaussian noise. Noise analysis of the HT reduces to a special case of this general analysis. The study is based on the statistical characteristics of the phase estimation. The Cramer-Rao bound, which was missing in the treatment of the HT in [13], is included to know the limitations of the phase estimator and to present better comparison between the time-delay and Hilbert transform. This comparison is based on considering an ideal Hilbert transformer that gives exactly -90^o phase shift without phase or amplitude distortion or other practical problems associated with the HT implementation.

In the next section the joint probability density function (pdf) of the input signal and its time-delayed (or: phase-shifted) version is derived in additive Gaussian noise, from which the pdf of the phase estimator is obtained and analyzed under various values of the effective parameters: the phase shift ψ, the true phase value ϕ, and the signal-to-noise ratio SNR.

4.2 Statistical Behavior of HT and Time-Delay in i.i.d. Additive Gaussian Noise

4.2.1 Input-Output Relationships in the Presence of Noise

For sinusoidal signals we have the relationship $\mathcal{H}(\cos(\omega t)) = \sin(\omega t)$. The input and the output of the time-delay are given under noise-free condition by $x(t) = A\,\sin(\omega t + \psi)$ and $y(t+\tau) = A\,\sin(\omega t)$, where A is the signal amplitude and $\psi = \omega\tau$ is the signal-dependent phase shift. In a causal system we have the following range of ψ

$$0 \;<\; f[\psi] \;< \pi \tag{4.5}$$

where

$$f[\psi] = -\pi + \{(\psi + \pi) \text{ modulo } (2\pi)\} \tag{4.6}$$

In the presence of noise the input-output relationships become

$$x(t) \;=\; A\,\sin(\phi(t) + \psi) + n(t) \tag{4.7}$$

$$y(t+\tau) \;=\; A\,\sin(\phi(t)) + n'(t) \tag{4.8}$$

where $\phi(t) = wt$, $n(t)$ is assumed to be Gaussian noise of zero mean and variance σ_n^2, and $n'(t)$ is the time-delayed version of $n(t)$. Apparently $n'(t)$ is also Gaussian with the same mean and variance as $n(t)$. It follows that $x(t)$ and

$y(t)$ are also Gaussian random variables with variance σ_n^2 and ensemble means given at any time instant t by

$$\begin{aligned} \mathrm{E}[x(t)] &= A\sin(\phi(t)+\psi) && (4.9)\\ \mathrm{E}[y(t+\tau)] &= A\sin(\phi(t)) && (4.10) \end{aligned}$$

In the presence of noise both $x(t)$ and its phase-shifted version $y(t+\tau)$ are random both in amplitude and in phase. To find the pdf of the random phase of $x(t)$ and $y(t+\tau)$ and its relationship to the deterministic phase at any time instant t, we should first write the sample functions $x(t)$ and $y(t+\tau)$ in terms of two new sample functions $R(t)$ (for amplitude) and $\epsilon(t)$ (for phase) such that the sample functions $x(t)$ and $y(t)$ maintain the same relationship between them as in the deterministic (noise-free) case. This gives in the case of time-delay (τ) the following transformations

$$\begin{aligned} x(t) &= R(t)\sin\big(\epsilon(t)+\psi\big) && (4.11)\\ y(t+\tau) &= R(t)\sin\big(\epsilon(t)\big) && (4.12) \end{aligned}$$

This is the same assumption made in reference [13] for the Hilbert transformer case. It is equivalent to defining a set of two new random variables (R,ϵ) in terms of the original random variables (x,y) according to the mappings f_1 and f_2 defined by

$$R = f_1(x,y) = \frac{x-\cos(\psi)y}{\sin(\psi)\cos\left(\mathrm{Tan}^{-1}\left\{\dfrac{\sin(\psi)}{1-\dfrac{y}{x}\cos(\psi)}\right\}\right)}$$

and

$$\epsilon = f_2(x,y) = f\left[\mathrm{Tan}^{-1}\left\{\frac{\sin(\psi)}{1-\dfrac{y}{x}\cos(\psi)}\right\}\right]$$

where $f[.]$ is defined in (4.6) and Tan^{-1} is the four-quadrant inverse tangent. The above choice of the relationships between (R,ϵ) and (x,y) makes sense when a comparison is made between the noise-free and noisy expressions for the original variables x and y in terms of amplitude and phase. This comparison constitutes the basis of this work. Figure 4.1 summarizes these relationships for HT and time-delay.

4.2.2 Joint PDF of the Amplitude and Phase Random Variables

In this analysis we concentrate on the discrete case and assume that the discrete noise process $\{n(k)\}$ is a sequence of i.i.d. (independent and identically

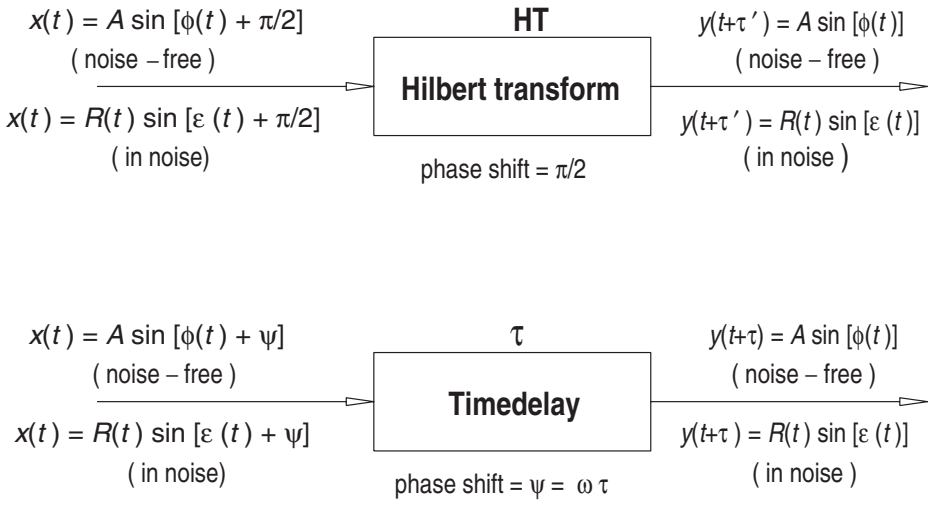


Figure 4.1: Input-output relationships for Hilbert transformer and time-delay τ under noise-free and noise conditions. $R(t)$ is the amplitude random variable, $\epsilon(t)$ is the phase random variable, and ω is the input radian frequency. $\tau^{'}$ is the practical delay caused by FIR implementation of HT.

distributed) Gaussian random variables. It follows that the phase shifted noise process $\{n^{'}(k)\}$ is also a sequence of i.i.d. Gaussian random variables with same mean and variance, and that the two random variables $\{n(k)\}$ and $\{n^{'}(k)\}$ are independent at any sampling instant k. Hence the discrete versions of x and y in (4.7) and (4.8) are also independent Gaussian random variables at any sampling instant k with joint probability density function (pdf) given at any sampling instant k by

$$g_{\psi,\phi}(x,y) = \frac{1}{2\pi\sigma_n^2} \exp\Big[-\frac{1}{2\sigma_n^2}\Big\{\big(x - A\ \sin(\phi+\psi)\big)^2 + \big(y - A\ \sin(\phi)\big)^2\Big\}\Big] \tag{4.13}$$

where for simplicity x, y, ϕ, R, and ϵ will be used to represent $x(k)$, $y(k+\tau)$, $\phi(k)$, $R(k)$, and $\epsilon(k)$ respectively.

In the presence of noise the relationship between x and its phase-shifted version y in terms of the amplitude and phase random variables R and ϵ would

be as in (4.11) and (4.12). Hence the joint pdf of R and ϵ is given by [74]

$$\begin{aligned} P_{\psi,\phi}(R,\epsilon) &= g_{\psi,\phi}\big(R\ \sin(\epsilon+\psi), R\ \sin(\epsilon)\big) \\ &\times \begin{vmatrix} \sin(\epsilon+\psi) & R\ \cos(\epsilon+\psi) \\ \sin(\epsilon) & R\ \cos(\epsilon) \end{vmatrix} \end{aligned} \tag{4.14}$$

where $g_{x,y}$ is given by (4.13) with x and y written in terms of R and ϵ as in (4.11) and (4.12).

4.2.3 PDF of the Phase Random Variable

In this chapter we concentrate on phase estimation rather than amplitude estimation. The pdf of the phase random variable ϵ is given by

$$p_{\psi,\phi}(\epsilon) = \int_0^\infty P_{\psi,\phi}(R,\epsilon)\ dR \tag{4.15}$$

which can be given, after some trigonometric manipulations, in the following functional form

$$\begin{aligned} p_{\psi,\phi}(\epsilon) &= h'_\psi(\epsilon) \\ &\times \Bigg[\frac{1}{2\pi}\exp\{-\mu_{\psi,\phi}\alpha\} + \sqrt{\frac{\mu_{\psi,\phi}\alpha}{\pi}}\cos\big(H_{\psi,\phi}(\epsilon)\big) \\ &\times \exp\{-\mu_{\psi,\phi}\alpha\ \sin^2\big(H_{\psi,\phi}(\epsilon)\big)\} \\ &\times \Big(\frac{1}{2} + \mathrm{erf}\{\sqrt{2\mu_{\psi,\phi}\alpha}\ \cos\big(H_{\psi,\phi}(\epsilon)\big)\}\Big)\Bigg] \end{aligned} \tag{4.16}$$

where

$$\alpha = A^2/2\sigma_n^2\ \ (\mathrm{signal-to-noise\ ratio}) \tag{4.17}$$

$$h_\psi(\epsilon) = f[\mathrm{Tan}^{-1}\{\frac{\sin(\epsilon)}{\sin(\epsilon+\psi)}\}] \tag{4.18}$$

$$h'_\psi(\epsilon) = \frac{dh_\psi(\epsilon)}{d\epsilon} = \frac{\sin(\psi)}{\sin^2(\epsilon)+\sin^2(\epsilon+\psi)} \tag{4.19}$$

$$\mu_{\psi,\phi} = \frac{\sin(\psi)}{h'_\psi(\phi)} \tag{4.20}$$

$$H_{\psi,\phi}(\epsilon) = h_\psi(\epsilon) - h_\psi(\phi) \tag{4.21}$$

$$\mathrm{erf}(x) = \frac{1}{\sqrt{2\pi}}\int_0^x e^{-t^2/2}dt \tag{4.22}$$

and $f[.]$ is defined in (4.6). Note that Tan^{-1} is the four-quadrant inverse tangent. It is clear that $p_{\psi,\phi}(\epsilon)$ is non-Gaussian. For high values of SNR, $p_{\psi,\phi}(\epsilon)$ can be approximated by

$$\begin{aligned} p_{\psi,\phi}(\epsilon) &= h_{\psi}^{'}(\epsilon)\sqrt{\frac{\mu_{\psi,\phi}\alpha}{\pi}}\cos\big(H_{\psi,\phi}(\epsilon)\big) \\ &\quad \times \exp\{-\mu_{\psi,\phi}\alpha\,\sin^2\big(H_{\psi,\phi}(\epsilon)\big)\} \\ &\quad \times \Big(\frac{1}{2}+\mathrm{erf}\{\sqrt{2\mu_{\psi,\phi}\alpha}\,\cos\big(H_{\psi,\phi}(\epsilon)\big)\}\Big) \end{aligned} \tag{4.23}$$

The above approximation can be used even for as low values of SNR as 1 dB, but the minimum value of $p_{\psi,\phi}(\epsilon)$ would be slightly negative; and this has no effect on the general shape of $p_{\psi,\phi}(\epsilon)$.

If $\psi = \pi/2$, we have $h_{\psi}^{'}(\epsilon) = 1$, $H_{\psi,\phi}(\epsilon) = f[\epsilon] - f[\phi] = \epsilon - \phi$ in the principal interval $(-\pi, \pi)$, and $\mu_{\psi,\phi} = 1$ $\big($see (4.18) - (4.21)$\big)$, hence (4.16) reduces to the Hilbert transform case obtained in [13] in a context of DPLLs

$$\begin{aligned} p_{\psi,\phi}(\epsilon) &= \frac{1}{2\pi}\exp(-\alpha) + \sqrt{\frac{\alpha}{\pi}}\cos(\epsilon-\phi)\exp\{-\alpha\sin^2(\epsilon-\phi)\} \\ &\quad \times \Big(\frac{1}{2}+\mathrm{erf}\{\sqrt{2\alpha}\,\cos(\epsilon-\phi)\}\Big) \end{aligned} \tag{4.24}$$

Note that $p_{\psi,\phi}(\epsilon)$ for HT is symmetric about $\epsilon = \phi$ with a peak that depends only on SNR. In this case, the function $p_{\psi,\phi}(\epsilon) = z_{\psi}(\phi, \epsilon)$, which is periodic in ϵ for each ϕ with a period of 2π, has its peak exactly along the lines $\epsilon = f[\phi] + 2m\pi$ in the (ϕ, ϵ) plane (for all integer m). This peak has a maximum value that is constant for a given SNR. In the general case (time-delay case) the peaks are slightly biased from $\epsilon = f[\phi] + 2m\pi$ and have variable maximum value depending on SNR, ψ, and the true value of the phase, $f[\phi]$. The bias of the pdf peak decreases as SNR increases or ψ approaches $\pi/2$. It is worth noting that this bias of the pdf peak at any ϕ does not mean that the expected value of the phase random variable ϵ is shifted by the same amount from the true value of the phase, $f[\phi]$, since this pdf is non-symmetric. In fact, the expected value of $\epsilon - f[\phi]$ is nearly zero for any ϕ when SNR is not very low, as will be shown in Subsection (4.2.5). The 2-D plot of $p_{\psi,\phi}(\epsilon)$ for SNR=10 dB and $\psi = \pi/3$ is shown in Figure 4.2 along with the contour plot to reveal the approximate symmetry about the line $\epsilon = \phi$ in the (ϕ, ϵ) plane.

4.2.4 PDF of the Phase Noise

From the above subsection we conclude that in the principal interval $(-\pi, \pi)$, the phase ϵ can be generally decomposed into a deterministic term $f[\phi]$ and a random variable η as follows

$$\epsilon = f[\phi] \; + \; \eta \tag{4.25}$$

where η is in the interval $(-\pi - f[\phi], \pi - f[\phi])$. This is similar to the result obtained for the Hilbert transformer [13] when the phase shift was $\pi/2$. The pdf of the phase noise η is given by

$$\rho_{\psi,\phi}(\eta) = p_{\psi,\phi}(\epsilon - f[\phi]) \tag{4.26}$$

which is generally dependent on ψ and $f[\phi]$ when the phase shift $\psi \neq \pi/2$. We can obtain this pdf from $p_{\psi,\phi}(\epsilon)$ for any value of ψ and ϕ by the intersection with the suitable plane.

The intersection of a plane ϕ = constant with $p_{\psi,\phi}(\epsilon)$ is symmetric when $\psi = \pi/2$ (HT case), while it is non-symmetric for general ψ except for high SNR. This can be seen in Figure 4.2. Although the contour plot is approximately symmetric about $\epsilon = \phi$, its boundaries are slightly varying, not straight parallel lines, giving non-symmetry when a plane ϕ = constant intersects the $p_{\psi,\phi}(\epsilon)$ plot. As SNR increases, the boundaries of the contour plot approach straight parallel lines and consequently $p_{\psi,\phi}(\eta)$ becomes symmetric. Figure 4.3 shows $\rho_{\psi,\phi}(\eta)$ when $f[\phi] = 0$ for different values of SNR ($\psi = \pi/3$) and different values of ψ (SNR = 10 dB). Only the principal period $(-\pi, \pi)$ is considered. It is clear that $\rho_{\psi,\phi}(\eta)$ is more symmetric and concentrated around $\eta = 0$ for higher values of SNR.

From (4.16) and (4.26) it is possible to show that $\rho_{\psi,\phi}(\eta)$ has the following anti-symmetry in the interval $(-\pi, \pi)$

$$\rho_{\psi,\phi}(\eta) = \rho_{\pi-\psi,\phi}(-\eta) \tag{4.27}$$

This anti-symmetry is clarified in Figure 4.3.

4.2.5 Expectation and Variance of the Phase Noise

The expected value and the variance of the phase noise η when $f[\phi] = 0$ are shown in Figure 4.4 for different values of ψ and SNR. Note that the symmetry in the expected value and the similarity in the variance result from the anti-symmetry in (4.27). For this value of $f[\phi]$ the Hilbert transform case ($\psi = \pi/2$) gives the minimum variance, but this is not always true for the whole range of $f[\phi]$. Figure 4.5 shows the expected value and the variance of the phase noise η for $\psi = \pi/3$ and different values of $f[\phi]$ as compared to the HT case. The HT phase pdf is ϕ-independent and give the same plots for the absolute expectation (which is zero) and the variance of the phase noise η for all values of $f[\phi]$. For the time-delay with any value of ψ, changing the value of $f[\phi]$ would result in changing the maximum of $\rho_{\psi,\phi}(\eta)$. This difference results in a slight difference

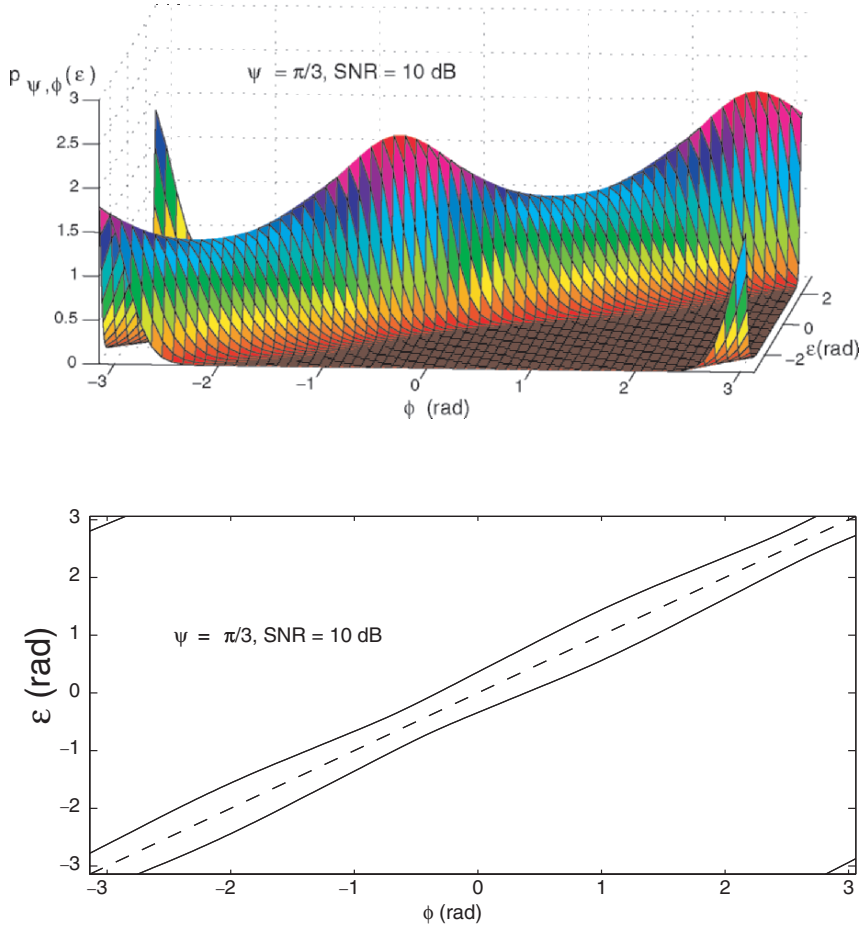


Figure 4.2: Above: the probability density function of the phase random variable, $p_{\psi,\phi}(\epsilon) = z_\psi(\phi, \epsilon)$, for $\psi = \pi/3$ and SNR = 10 dB. Below: contour plot of the above $p_{\psi,\phi}(\epsilon)$ at the level of 0.5 for one period in the (ϕ, ϵ) plane. Dotted line is the $\epsilon = \phi$ line. It is clear that $p_{\psi,\phi}(\epsilon)$ is nearly symmetric about $\epsilon = \phi$ line. As SNR increases, the contour plot becomes two parallel lines.

in the expected value and the variance of η for different values of $f[\phi]$ as shown in Figure 4.5 for $\psi = \pi/3$ and different values of $f[\phi]$. For some values of $f[\phi]$ the variance can go below the HT case. However, the performance is measured by considering the expectation and the variance of η for the whole range of $f[\phi]$. Therefore the (ideal) Hilbert transformer outperforms the time-delay in all cases.

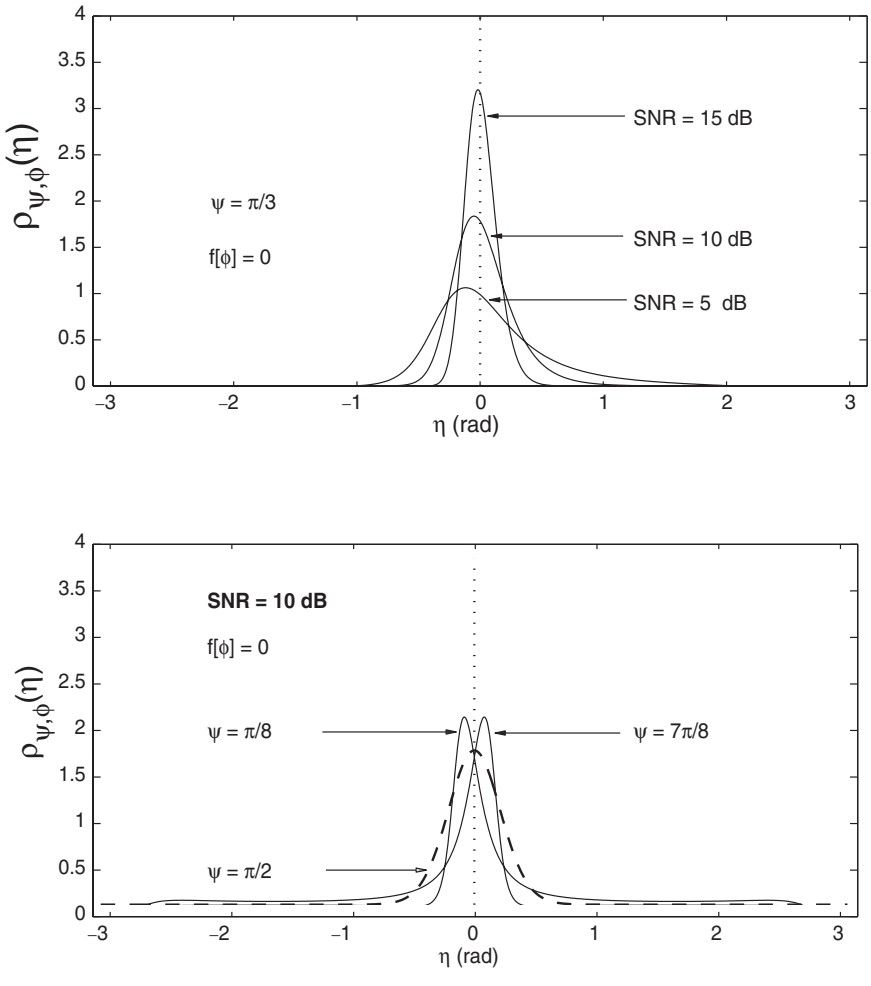


Figure 4.3: The probability density function $\rho_{\psi,\phi}(\eta)$ of the phase noise η when $f[\phi] = 0$. Above: $\rho_{\psi,\phi}(\eta)$ for $\psi = \pi/3$ and different values of SNR. Below: $\rho_{\psi,\phi}(\eta)$ for SNR $=$ 10 dB and different values of ψ. Note that the dashed curve ($\psi = \pi/2$) is symmetric and represents the Hilbert transform (HT) case. The two solid curves clarify the ψ anti-symmetry of the phase noise pdf.

Note that this comparison is based on considering an ideal Hilbert transformer that gives exactly -90^o phase shift without phase or amplitude distortion or other practical problems associated with the implementation [61, 60].

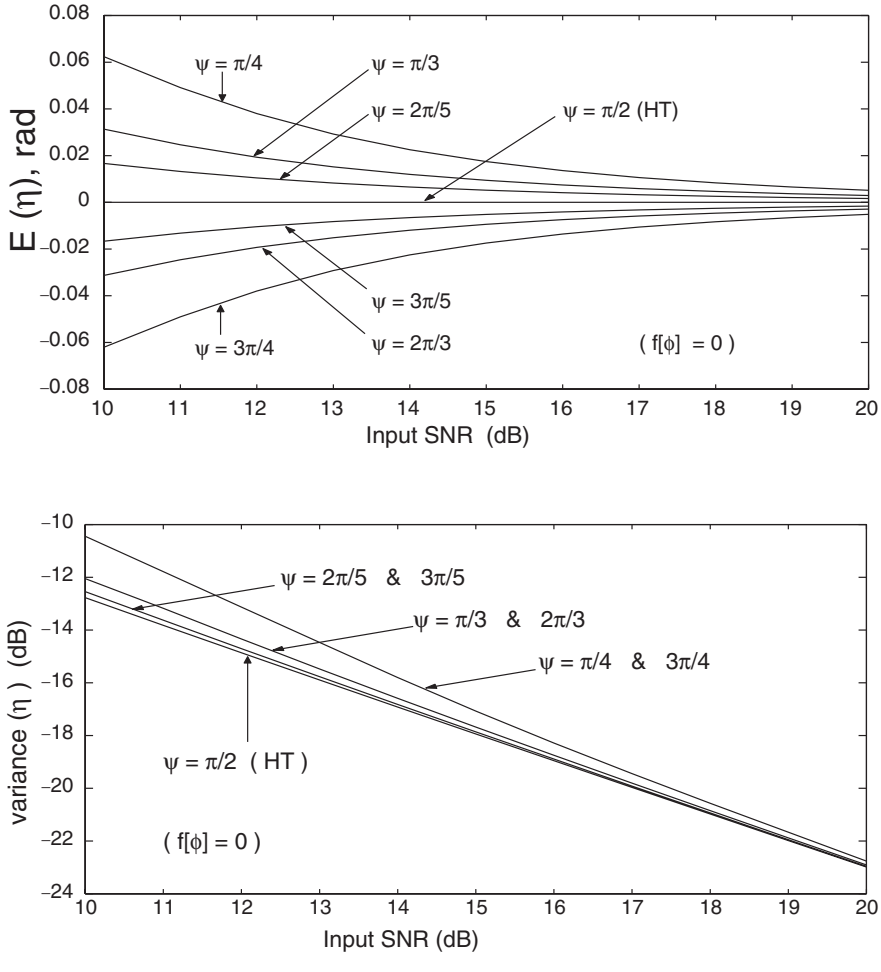


Figure 4.4: The expected value (above) and the variance (below) of the phase noise η for different values of ψ and SNR ($f[\phi] = 0$). The case $\psi = \pi/2$ is the Hilbert transform (HT) case which gives minimum value for the variance and the absolute expectation (approximately zero) of the phase noise η. The symmetry of the expected value about zero and the similarity of the variance for ψ and $\pi - \psi$ cases are due to the ψ anti-symmetry of the phase noise pdf.

In all the cases studied above for the time-delay, the expected value of the phase noise η is approximately zero and decreases when SNR increases, also the variance decreases substantially when SNR increases.

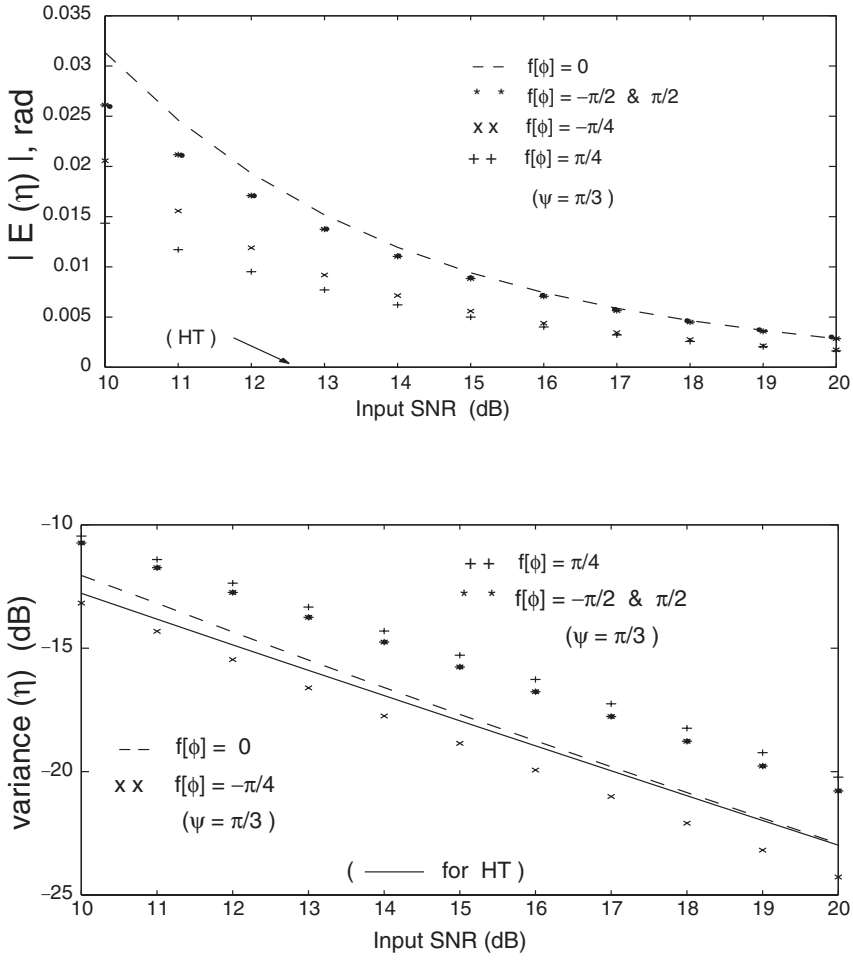


Figure 4.5: The expected value (above) and the variance (below) of the phase noise η for different values of $f[\phi]$ and SNR when $\psi = \pi/3$. The solid line represents the HT case which is ϕ-independent.

4.2.6 The phase Estimator and Ranges of Cramer-Rao Bounds

From the above analysis, the random phase variable ϵ can be used as a phase estimator, $\hat{\phi}$. It can be expressed in the interval $(-\pi, \pi)$ in terms of ψ, x, and

y according to (4.11) and (4.12) as follows

$$\epsilon \;=\; \hat{\phi} \;=\; f\left[\mathrm{Tan}^{-1}\left\{\frac{\sin(\psi)}{1-\dfrac{y}{x}\cos(\psi)}\right\}\right] \tag{4.28}$$

where $f[.]$ is defined in (4.6) and Tan^{-1} is the four-quadrant inverse tangent.

Since $\hat{\phi}$ is approximately unbiased for reasonable values of SNR (a minimum of 10 dB is acceptable in all cases), its variance is lower-bounded by the Cramer-Rao (CR) bound [75], which can be expressed in this case as follows

$$\begin{aligned}\mathrm{var}(\hat{\phi}) \;&=\; \mathcal{E}(\epsilon-\phi)^2 \geq \frac{1}{\mathcal{E}\Big\{\Big[\dfrac{\partial \ln\{p_{\psi,\phi}(\epsilon)\}}{\partial\phi}\Big]^2\Big\}} \\ &=\; \frac{1}{\displaystyle\int_{-\pi-f[\phi]}^{\pi-f[\phi]}\Big[\frac{\partial \ln\{p_{\psi,\phi}(\epsilon)\}}{\partial\phi}\Big]^2 p_{\psi,\phi}(\epsilon)\,d\epsilon} \;=\; \mathrm{CR}_\psi(\phi)\end{aligned} \tag{4.29}$$

There is no analytic expression for the CR bound $\mathrm{CR}_\psi(\phi)$, hence it should be found numerically using (4.29) and (4.16). Figure 4.6 shows the variance of the time-delay phase estimator $\mathrm{var}(\hat{\phi})$ and its CR bound for $\psi = \pi/3$ and $f[\phi] = 0$. The variance converges to its CR bound as SNR increases. This is true for all values of $\psi = \pi/3$ and $f[\phi]$. For HT, the variance of the phase estimator, $\mathrm{var}(\hat{\phi})$, is nearly identical with the CR bound in the range of SNR shown in Figure 4.6.

Figure 4.6 also shows the approximate ranges of CR bounds of the time-delay phase estimator when $\psi = \pi/7$ & $6\pi/7$ (the area between dotted lines) and $\psi = \pi/3$ & $2\pi/3$ (the area between dashed lines) as $f[\phi]$ ranges throughout the interval $(-\pi, \pi]$. The range is found numerically for each ψ by calculating CR bounds for all values of $f[\phi]$ in the principal interval $-\pi \;<\; f[\phi] \;\leq\; \pi$. Similarity in CR bounds between ψ and $\pi - \psi$ cases is due to the ψ anti-symmetry of $p_{\psi,\phi}$ discussed earlier. The solid line represents CR bound of the HT phase estimator, which is independent of the phase true value $f[\phi]$. As ψ approaches $\pi/2$, the range of CR bounds approaches the HT case.

The performance of the time-delay for each ψ is measured by considering the least upper bound $\{\mathrm{CR}_\psi(\phi) \mid -\pi \;<\; f[\phi] \;\leq\; \pi\}$. As such the (ideal) Hilbert transformer outperforms the time-delay in all cases.

It is clear that the performance of the time-delay phase estimator, regarding both the expectation and the variance of the phase noise, decreases as ψ goes far from $\pi/2$, especially for low SNR. Hence if a constant time-delay τ is to replace the Hilbert Transform in some signal processing system while keeping highest possible performance in the presence of noise, the appropriate choice of

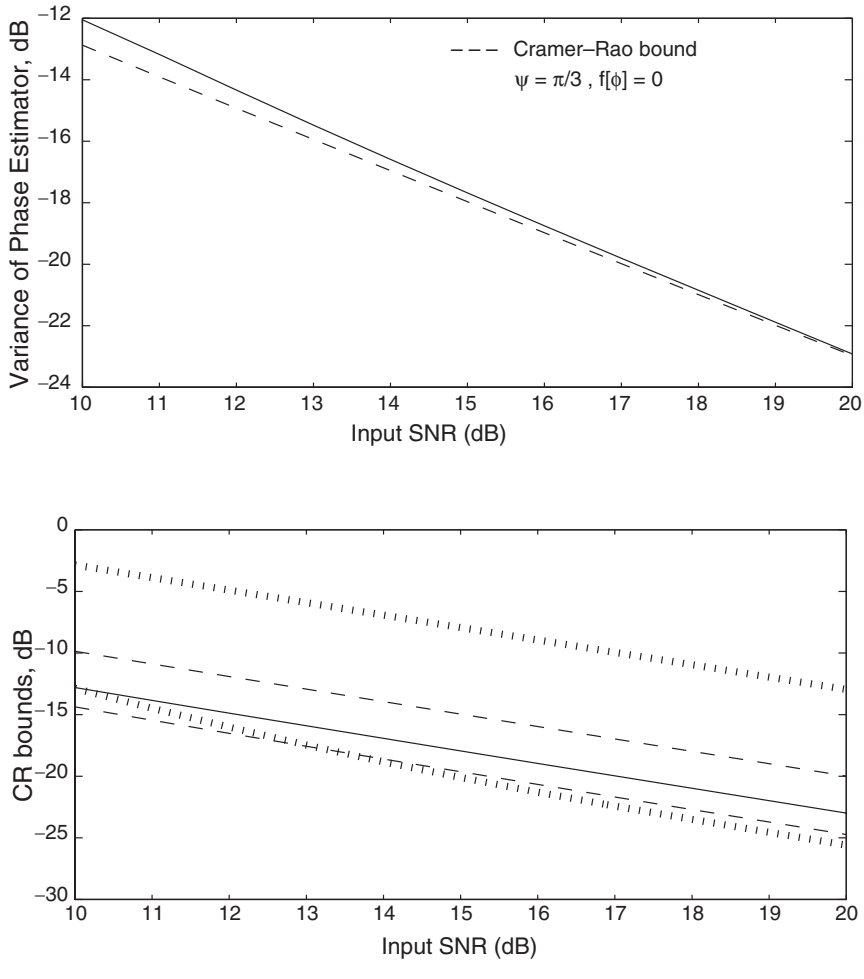


Figure 4.6: Above: the variance and the Cramer-Rao bound of the time-delay phase estimator for $\psi = \pi/3$ and $f[\phi] = 0$. The variance converges to the CR bound as SNR increases. Below: approximate ranges of the CR bounds of the time-delay phase estimator for $\psi = \pi/7$ & $6\pi/7$ (the area between dotted lines), and $\psi = \pi/3$ & $2\pi/3$ (the area between dashed lines). The range is found numerically for each ψ by calculating the CR bounds for all values of $f[\phi]$ in the principal interval $-\pi < f[\phi] \leq \pi$. Similarity in the CR bounds between ψ and $\pi - \psi$ is due to the ψ anti-symmetry of the phase pdf. The solid line represents the CR bound of the HT phase estimator, which is independent of the phase true value $f[\phi]$. As ψ approaches $\pi/2$, the range of the CR bounds approaches the HT case.

τ would be application dependent. The proper value of τ should keep $\psi = \omega\tau$ as near to $\pi/2$ as possible throughout the expected range of the input frequencies. However, this condition on the choice of τ becomes less strict as SNR increases. Also the performance regarding the expected value of the phase can be made the same as in the HT case by utilizing a phase transformation that makes the phase pdf symmetric as shown in the following subsection.

4.2.7 A Symmetric Transformation

As shown above, the pdf of the phase estimator ϵ is non-symmetric. However, this pdf can be transformed into a symmetric pdf by the following transformation of the random variable ϵ

$$\xi \;=\; h_\psi(\epsilon) \;=\; f\left[\mathrm{Tan}^{-1}\left\{\frac{\sin(\epsilon)}{\sin(\epsilon+\psi)}\right\}\right] \tag{4.30}$$

From (4.6) and (4.19) we can deduce that both the numerator and the denominator of $h^{'}(\epsilon) = dh(\epsilon)/d\epsilon$ are positive. Therefore $h^{'}(\epsilon)$ is always positive and $h(\epsilon)$ is monotonically (in fact: strictly) increasing in the principal interval $(-\pi, \pi)$. Hence the pdf of ξ can be given by [74]

$$\mathbf{p}_{\psi,\phi}(\xi) = p_{\psi,\phi}\big(h_\psi^{-1}(\xi)\big)\left|\frac{d\epsilon}{d\xi}\right| \tag{4.31}$$

From (4.16), (4.21), (4.30), and (4.31) we obtain

$$\begin{aligned}\mathbf{p}_{\psi,\phi}(\xi) \;=\; & \frac{1}{2\pi}\exp\{-\mu_{\psi,\phi}\alpha\} + \sqrt{\frac{\mu_{\psi,\phi}\alpha}{\pi}}\cos\big(\xi - h_\psi(\phi)\big) \\ & \times \exp\{-\mu_{\psi,\phi}\alpha\,\sin^2\big(\xi - h_\psi(\phi)\big)\} \\ & \times \left(\frac{1}{2} + \mathrm{erf}\{\sqrt{2\mu_{\psi,\phi}\alpha}\,\cos\big(\xi - h_\psi(\phi)\big)\}\right)\end{aligned} \tag{4.32}$$

which is symmetric about $\xi = h_\psi(\phi)$, hence $\xi - h_\psi(\phi)$ has zero expected value irrespective of ϕ and ψ. Therefore ξ can be decomposed as follows

$$\xi = \Phi + \nu \tag{4.33}$$

where $\Phi = h_\psi(\phi)$ is the deterministic transformed phase and ν is a non-Gaussian phase noise with zero mean. However, the variance of ξ is still dependent on ψ and ϕ. Numerical calculations showed that, for every value of ψ, the l.u.b of the CR bounds of ξ converges for reasonable SNR's to that of ϵ discussed in the previous subsection. If ψ is not far from $\pi/2$, these two l.u.b.'s are nearly identical. Hence ideal improvement in the expectation and no improvement in

the variance of the phase estimator are obtained by this transformation. Since the mapping $h_\psi : \phi \rightarrow \Phi$ is one-valued and strictly increasing in the principal interval of ϕ (i.e. $(-\pi, \pi)$), h_ψ^{-1} is also one-valued in the principal interval $(-\pi, \pi)$ [76]. Hence there is no ambiguity in transforming (4.32) in terms of Φ (rather than ϕ) as long as we consider a period of 2π. The actual expression of h_ψ^{-1} can be given after some manipulations in the following form

$$\phi = h_\psi^{-1}(\Phi) = \begin{cases} a & b \ \sin(\Phi) \geq 0 \\ f[a + \pi] & \text{otherwise.} \end{cases} \tag{4.34}$$

where

$$b = \frac{\sin(\psi)\tan(\Phi)}{1 - \cos(\psi)\tan(\Phi)} \tag{4.35}$$

$$a = \tan^{-1}(b) \tag{4.36}$$

and $f[.]$ is defined in (4.6). The function $\tan^{-1}$ is the ordinary inverse tangent.

The function $h_\psi(.)$ defined in (4.18) was originally proposed as the characteristic function of the phase error detector of a new DPLL, the time-delay digital tanlock loop (TDTL), in an attempt to replace the HT by a time-delay in DPLLs [70, 71] (see also Chapter 3). However, it appears form the analysis in this chapter that this function has an inherent relationship to the statistical behavior of the time-delay in the presence of Gaussian noise.

For TDTL, this symmetric transformation of the phase random variable would result in high performance of the TDTL in the presence of noise that is essentially equivalent to the performance when HT is utilized for reasonable values of SNR.

Hence if it is possible to replace a HT by a time-delay τ (as a phase-shifter) with the above phase transformation in some signal processing system (like in DPLLs), the choice of τ would be mainly related to the noise-free performance of the system, especially for high SNR.

4.3 Conclusions

A time-delay has been introduced in Chapter 3 as a substitute for the Hilbert transformer (HT) in digital phase-locked loops (DPLLs) for the purpose of phase shifting. This resulted in a major reduction in the system complexity. This chapter has shown that if this replacement is possible under noise-free conditions in some signal processing system, it would also be successful in the presence of additive Gaussian noise. For sinusoidal signals, the performance of a time-delay τ (which produces a signal-dependent phase-shift $\psi = \omega\tau$, ω being the signal radian frequency) is comparable to the performance of a Hilbert transformer (which produces a signal-independent 90^o phase-shift) in the presence of independent and identically distributed (i.i.d.) additive Gaussian noise. The

performance of the time-delay approaches that of Hilbert transformer for high signal-to-noise ratios (SNRs) and the proper choice of τ. In case τ is constant and a range of ω is expected, the performance of the time-delay is best when τ is chosen to keep the range of ψ as near as possible to $\pi/2$ throughout the expected range of the input frequencies. However, this condition on the choice of τ becomes less strict as SNR increases. Also, the performance regarding the expected value of the phase can be made the same as in the HT case by utilizing a proposed phase transformation that makes the phase probability density function (pdf) symmetric. The criterion used in this analysis is the effect of noise on the phase of the input signal and its time-delayed (or: phase-shifted) version such that similar relationship between them is maintained as in the noise-free case. In additive Gaussian noise the time-delay phase estimator can be approximated by the noise-free phase plus a non-Gaussian phase noise. The pdf of the phase noise in the case of time-delay is non-symmetric with a peak that depends on ψ, the deterministic phase ϕ, and SNR. However, as SNR increases, the expected value of the time-delay phase estimator approaches the true phase value and its variance substantially decreases and converges to the Cramer-Rao bound for all ranges of the effective parameters: the phase shift ψ, the true phase value ϕ, and the signal-to-noise ratio SNR.

Chapter 5

The Time-delay Digital Tanlock Loop in Noise

5.1 Introduction

In Chapter 3, a constant time-delay unit is used to produce a phase-shifted version of the incoming signal, giving rise to the time-delay digital tanlock loop (TDTL) [70, 71]. This method reduces the complexity of the phase-shifter and avoids the limitations and other problems that accompanies the 90^o phase-shifter in the conventional DTL (CDTL) [13]. The main advantages of CDTL are maintained by TDTL despite its reduced structure (see Chapter 3).

In Chapter 4, we analyzed the performance of the time-delay, which produces a signal-dependent phase shift, in the presence of additive Gaussian noise. We compared its performance with that of the (ideal) Hilbert transformer. The result is of general interest in signal processing.

In this chapter we analyze the performance of the first- and second-order TDTLs in the presence of additive Gaussian noise [72]. Specifically, we investigate the effect of additive Gaussian noise on the sytem equation, the input and output of the phase error detector, locking conditions, and the steady-state phase errors. It is shown that, in the presence of additive Gaussian noise, the phase at the output of the phase error detector (PED) can be represented by the noise-free phase plus a non-Gaussian phase errors. Cramer-Rao bound, which was missing in the treatment of CDTL in [13], is included in this study for better understanding of the circuit performance. The mean value of the steady-state phase errors at the input and the output of the phase error detector are shown to be the same as the noise-free steady-state phase errors ϕ_{ss} and e_{ss}, respectively, while the variance decreases as the signal-to-noise ratio (SNR) increases and converges to the Cramer-Rao bound for all values of the effective parameters: ψ, $K_1^{'}$, and SNR. The locking ranges of the circuit parameters are

the same as those under noise-free conditions. The best possible performance can be ensured in TDTL design when the time-delay τ is chosen to give a phase shift $\psi = \omega\tau$ as near as possible to $\pi/2$ from both sides during the expected range of the input frequency ω.

5.2 Noise Analysis of the TDTL

In this section we investigate the effect of additive Gaussian noise on the performance of the first- and second-order TDTLs.

5.2.1 System Equation

The noise-free system analysis was given in Chapter 3. Here we present the main equations in the presence of additive Gaussian noise. The loop accepts a sinusoidal input signal $y(t)$ having a radian frequency ω with a frequency offset $\Delta\omega(= \omega - \omega_o)$ from the nominal radian frequency ω_o of the digital clock. The input signal is given by

$$y(t) = A\sin[\omega_o t + \theta(t)] + n(t) \tag{5.1}$$

where A is the signal amplitude, $\theta(t)(= \Delta\omega t + \theta_o)$ is the phase process of the incoming signal, θ_o being a constant, and $n(t)$ is additive Gaussian noise with zero mean and variance σ_n^2.

The time-delay unit introduces a constant time-delay τ in the input signal which causes a phase lag $\psi(= \omega\tau)$ proportional to input radian frequency ω. The time-delayed version of the input signal, denoted by $x(t)$, can be expressed as

$$x(t) = A\sin[\omega_o t + \theta(t) - \psi] + n^{'}(t) \tag{5.2}$$

where $n^{'}(t)$ is the phase-shifted version of $n(t)$. At the k^{th} sampling instant, the sampled values of $y(t)$ and $x(t)$ are given respectively by

$$y(k) = A\sin[\omega_o t(k) + \theta(k)] + n(k) \tag{5.3}$$

$$x(k) = A\sin[\omega_o t(k) + \theta(k) - \psi] + n^{'}(k) \tag{5.4}$$

where $\theta(k) = \theta[t(k)]$, $n(k) = n(t(k))$, and $n^{'}(k) = n^{'}(t(k))$.

The sampling interval between the sampling instants $t(k)$ and $t(k-1)$ is given by

$$T(k) = \mathcal{T}_o - c(k-1) \tag{5.5}$$

where $\mathcal{T}_o(= \frac{2\pi}{\omega_o})$ is the nominal period of the digital clock and $c(i)$ is the output of the digital filter at the i^{th} sampling instant. Assuming $t(0) = 0$, the total

time $t(k)$ up to the k^{th} sampling instant is

$$t(k) = \sum_{i=1}^{k} T(i) = k\mathcal{T}_o - \sum_{i=0}^{k-1} c(i) \tag{5.6}$$

Thus, $y(k)$ and $x(k)$ can be written as

$$y(k) = A \sin\left[\theta(k) - \omega_o \sum_{i=0}^{k-1} c(i)\right] + n(k) \tag{5.7}$$

$$x(k) = A \sin\left[\theta(k) - \omega_o \sum_{i=0}^{k-1} c(i) - \psi\right] + n^{'}(k) \tag{5.8}$$

The phase error $\phi(k)$ is defined as [70, 71] (see also Chapter 3)

$$\phi(k) = \theta(k) - \omega_o \sum_{i=0}^{k-1} c(i) - \psi \tag{5.9}$$

Now $y(k)$ and $x(k)$ in the presence of additive Gaussian noise can be expressed as

$$y(k) = A \sin[\phi(k) + \psi] + n(k) \tag{5.10}$$

$$x(k) = A \sin[\phi(k)] + n^{'}(k) \tag{5.11}$$

The phase equation was given in Chapter 3 as follows

$$\phi(k+1) = \phi(k) - \omega c(k) + \Lambda_o \tag{5.12}$$

where $\Lambda_o = 2\pi\frac{\omega-\omega_o}{\omega_o}$. This is the general phase equation of TDTL based on the definition of phase error. Under noise-free conditions this leads to the results shown in Chapter 3. In the presence of noise, there would be phase noise in addition to the noise-free phase process. To find this noise we should analyze the effect of noise on the input and the output of the phase error detector.

5.2.2 Statistical Behavior of TDTL Phase Error Detector

Assuming that the sampled noise process $\{n(k)\}$ is a sequence of i.i.d. (independent and identically distributed) Gaussian random variables with zero mean and a variance of σ_n^2, it follows that the phase shifted noise process $\{n^{'}(k)\}$ is also a sequence of i.i.d. Gaussian random variables with same mean and variance, and that the two noise processes $\{n(k)\}$ and $\{n^{'}(k)\}$ are independent. Hence

y and x in (5.10) and (5.11) are also independent Gaussian random variables with joint probability density function (pdf) given at any sampling instant k by

$$g_{\psi,\phi}(x,y) = \frac{1}{2\pi\sigma_n^2}\exp\Big[-\frac{1}{2\sigma_n^2}\big((x - A\sin(\phi)\big)^2 + (y - A\sin(\phi+\psi)^2\big)\Big] \quad (5.13)$$

where for simplicity x, y, and ϕ are used to represent $x(k)$, $y(k)$, and $\phi(k)$, respectively.

In CDTL the characteristic function is linear and there is no phase transformation. Hence noise analysis at the input of the Phase Error Detector (PED) is sufficient [13]. For TDTL the characteristic function of the PED, (3.14) and (3.15) in Chapter 2, performs non-linear transformation of the input phase. Hence in the next two sub-subsections we will study the statistical behavior of the phase at the input and at the output of the PED separately.

A. Phase PDF at the Input of the PED

In the presence of noise both y and its phase-shifted version x would be random in amplitude and phase. To find the pdf of the random phase of y and x and its relationship to the deterministic phase, we should first write x and y in terms of two new random variables R (for amplitude) and ϵ (for phase) such that the random variables x and y keep the same relationship between them as in the deterministic case. This gives in the case of TDTL the following transformations

$$x = R\sin(\epsilon) \quad (5.14)$$

$$y = R\sin(\epsilon+\psi) \quad (5.15)$$

hence the joint pdf of R and ϵ is given by [74]

$$P_{\psi,\phi}(R,\epsilon) = g\big(R\sin(\epsilon), R\sin(\epsilon+\psi)\big)R\sin(\psi) \quad (5.16)$$

In DPLLs the concentration is on the phase rather than on the amplitude. The pdf of the input phase random variable ϵ is given by

$$p_{\psi,\phi}(\epsilon) = \int_0^\infty P_{\psi,\phi}(R,\epsilon)\, dR \quad (5.17)$$

which can be given in the following form

$$\begin{aligned} p_{\psi,\phi}(\epsilon) &= h'_{\psi}(\epsilon)\Big[\frac{1}{2\pi}\exp\{-\mu_{\psi,\phi}\alpha\} + \sqrt{\frac{\mu_{\psi,\phi}\alpha}{\pi}}\cos\big(H_{\psi,\phi}(\epsilon)\big) \\ &\quad \times \exp\{-\mu_{\psi,\phi}\alpha\sin^2\big(H_{\psi,\phi}(\epsilon)\big)\} \\ &\quad \times \left(\frac{1}{2} + \mathrm{erf}\{\sqrt{2\mu_{\psi,\phi}\alpha}\cos\big(H_{\psi,\phi}(\epsilon)\big)\}\right)\Big] \end{aligned} \quad (5.18)$$

where

$$\alpha = A^2/2\sigma_n^2 \ \text{(signal} - \text{to} - \text{noise ratio)} \tag{5.19}$$

$$h_\psi^{'}(\epsilon) = \frac{dh_\psi(\epsilon)}{d\epsilon} = \frac{\sin(\psi)}{\sin^2(\epsilon)+\sin^2(\epsilon+\psi)} \tag{5.20}$$

$$\mu_{\psi,\phi} = \frac{\sin(\psi)}{h_\psi^{'}(\phi)} \tag{5.21}$$

$$H_{\psi,\phi}(\epsilon) = h_\psi(\epsilon) - h_\psi(\phi) \tag{5.22}$$

$$\text{erf}(x) = \frac{1}{\sqrt{2\pi}}\int_0^x e^{-t^2/2}dt \tag{5.23}$$

and $f[.]$ is defined in (4.6). It is clear that $p_{\psi,\phi}(\epsilon)$ is non-Gaussian and periodic in ϵ and ϕ with periods of 2π. It is also non-symmetric about the plane $\epsilon = \phi$ for $\psi \neq \pi/2$. If $\psi = \pi/2$, we have $h_\psi^{'}(\epsilon) = 1$, $H_{\psi,\phi}(\epsilon) = f[\epsilon] - f[\phi] = \epsilon - \phi$ in the principal interval $(-\pi, \pi)$, and $\mu_{\psi,\phi} = 1$ $\big($see (5.19) - (5.22)$\big)$, hence (5.18) reduces to the Hilbert transform case obtained for CDTL in [13].

B. Phase PDF at the Output of the PED

Now the phase at the output of the phase error detector is also a non-Gaussian random variable ξ given by

$$\xi = h_\psi(\epsilon) = f\left[\text{Tan}^{-1}\left\{\frac{\sin(\epsilon)}{\sin(\epsilon+\psi)}\right\}\right] \tag{5.24}$$

where Tan^{-1} is the four-quadrant arctan function. In Chapter 3, the function $h_\psi(\epsilon)$ was shown to be continuous over the principal interval $(-\pi, \pi)$ (see Appendix, Chapter 3). Also we have $\frac{dh_\psi(\phi)}{d\phi} > 0$ since $0 < \sin(\psi) < 1$. Therefore $h_\psi(\phi)$ is monotonically increasing in the principal interval. Hence the pdf of ξ can be given by [74]

$$\mathbf{p}_{\psi,\phi}(\xi) = p_{\psi,\phi}\big(h_\psi^{-1}(\xi)\big)\left|\frac{d\epsilon}{d\xi}\right| \tag{5.25}$$

From (3.14), (5.18), (5.24), and (5.25) we obtain

$$\begin{aligned}\mathbf{p}_{\psi,\phi}(\xi) &= \frac{1}{2\pi}\exp\{-\mu_{\psi,\phi}\alpha\} + \sqrt{\frac{\mu_{\psi,\phi}\alpha}{\pi}}\cos\big(\xi - h_\psi(\phi)\big) \\ &\quad \times \exp\{-\mu_{\psi,\phi}\alpha\,\sin^2\big(\xi - h_\psi(\phi)\big)\} \\ &\quad \times \left(\frac{1}{2} + \text{erf}\big\{\sqrt{2\mu_{\psi,\phi}\alpha}\,\cos\big(\xi - h_\psi(\phi)\big)\big\}\right)\end{aligned} \tag{5.26}$$

which is periodic in ξ of period 2π. It has a maximum at $\xi = h_\psi(\phi)$, hence $\xi - h_\psi(\phi)$ has zero expected value irrespective of ϕ and ψ. Therefore ξ can be

decomposed as follows

$$\xi = e + \eta \tag{5.27}$$

where $e = h_\psi(\phi)$ is the deterministic transformed phase and η is a non-Gaussian phase noise with zero mean. If we consider ξ in the main interval $(-\pi, \pi)$, then the phase noise η lies in the interval $(-\pi - e, \pi - e)$. The pdf of the phase noise η can be given explicitly as follows

$$\begin{aligned}\rho_{\psi,e}(\eta) &= \frac{1}{2\pi}\exp(-m_{\psi,e}\alpha) + \sqrt{\frac{m_{\psi,e}\alpha}{\pi}}\cos(\eta)\exp\{-m_{\psi,e}\alpha\sin^2(\eta)\} \\ &\quad \times \left(\frac{1}{2} + \mathrm{erf}\{\sqrt{2m_{\psi,e}\alpha}\cos(\eta)\}\right)\end{aligned} \tag{5.28}$$

where

$$m_{\psi,e} = \mu_{\psi,h_\psi^{-1}(e)} \tag{5.29}$$

This pdf has a form similar to the result obtained for the CDTL [13], except for the additional factor $m_{\psi,e}$. This factor has no effect on the expected value of η which is always zero as in the CDTL case. However, the variance of η is now dependent on ψ and e. Using (5.22), (5.26), and (5.27) we have the following ψ symmetry

$$\rho_{\psi,e}(\eta) = \rho_{\pi-\psi,e}(\eta) \tag{5.30}$$

Since the mapping $h_\psi : \phi \to e$ is one-valued and strictly increasing in the principal interval of ϕ (i.e. $(-\pi, \pi)$), h_ψ^{-1} is also one-valued [76]. Hence there is no ambiguity in transforming the above pdfs in terms of e (rather than ϕ) as long as we consider a period of 2π. The actual expression of h_ψ^{-1} is similar to that of ϕ_{ss} given in (5.33) with ϕ_{ss} replaced by $h_\psi^{-1}(e)$. Figure 5.1 shows the 2-D plot of $\mathbf{p}_{\psi,\phi}(\xi)$ for $\psi = \pi/3$ and SNR = 10 dB and the contour plot of this pdf as compared to that of CDTL. Figure 5.2 shows $\rho_{\psi,e}(\eta)$ when $e = 0$ for different values of ψ and SNR.

5.2.3 Phase Estimation and Cramer-Rao Bounds

Since the random phase ξ at the output of the PED gives the deterministic phase e plus a phase noise as in (5.27), it can be used as a phase estimator $\hat{e}$. As $\eta = \xi - e$ has zero expected value for all ψ and ϕ, this estimator is unbiased

and therefore its variance $\mathrm{var}(\hat{e})$ is lower-bounded by the Cramer-Rao bound [75], which is given in this case by

$$\begin{aligned}
\mathrm{var}(\hat{e}) &= \mathcal{E}(\xi - e)^2 \\
&\geq \frac{1}{\mathcal{E}\left\{\left[\dfrac{\partial \ln\{\mathrm{p}_{\psi,h_\psi^{-1}(e)}(\xi)\}}{\partial e}\right]^2\right\}} \\
&= \frac{1}{\displaystyle\int_{-\pi-e}^{\pi-e}\left[\frac{\partial \ln\{\mathrm{p}_{\psi,h_\psi^{-1}(e)}(\xi)\}}{\partial e}\right]^2 \mathrm{p}_{\psi,h_\psi^{-1}(e)}(\xi)\, d\xi} \\
&= \mathrm{CR}_\psi(e) \qquad (5.31)
\end{aligned}$$

where $\mathcal{E}$ is the expectation functional. Since the mapping h_ψ^{-1} is one-valued in the principal interval as shown in the previous subsection, there is no ambiguity in evaluating the above integral as long as we consider a period of 2π.

Numerical calculations showed that the variance of ξ is approximately identical with the Cramer-Rao (CR) bound for reasonable values of SNR. Hence we will use CR bounds for the purpose of performance assessment and comparison.

It is evident from (5.31) that the CR bound is dependent on $\psi = \psi_o/W$, e, and SNR. Hence in TDTL case we expect ranges of CR bounds rather than single CR bound for CDTL. For every value of ψ, CR bound can go below the CDTL case for some values of e. However, for every ψ, the performance is measured by considering all the range of CR bounds for all possible e. In this case we consider the least upper bound $\{\mathrm{CR}_\psi(e) \mid -\pi < e \leq \pi\}$. Therefore the (ideal) CDTL outperforms TDTL in the presence of noise in all cases. As ψ approaches $\pi/2$, the range of CR bounds approach the (ideal) CDTL Cramer-Rao bound. Hence the difference in performance is less evident as ψ approaches $\pi/2$.

It follows that for the best possible performance in the presence of noise we should choose the time-delay τ such that we keep $\psi = \omega\tau$ as near as possible to $\pi/2$ throughout the expected range of ω which is supposed to be fit inside the locking range of TDTL for some value of $\psi_o = \omega_o\tau$ (that decides the value of ω_o) and a low value of K_1. The natural choice in this case is $\{(\omega_1+\omega_2)/2\}\tau = \pi/2$.

Figure 5.3 shows the ranges of CR bounds for different values of $\psi = \psi_o/W$ and SNR. It is apparent that the range of the CR bounds approaches the CDTL bound as ψ approaches $\pi/2$. According to the above performance measure, the (ideal) CDTL outperforms TDTL in the presence of noise in all cases when the variance is considered, while the performance is similar regarding the expected value of the phase error. However, the difference in performance is less evident

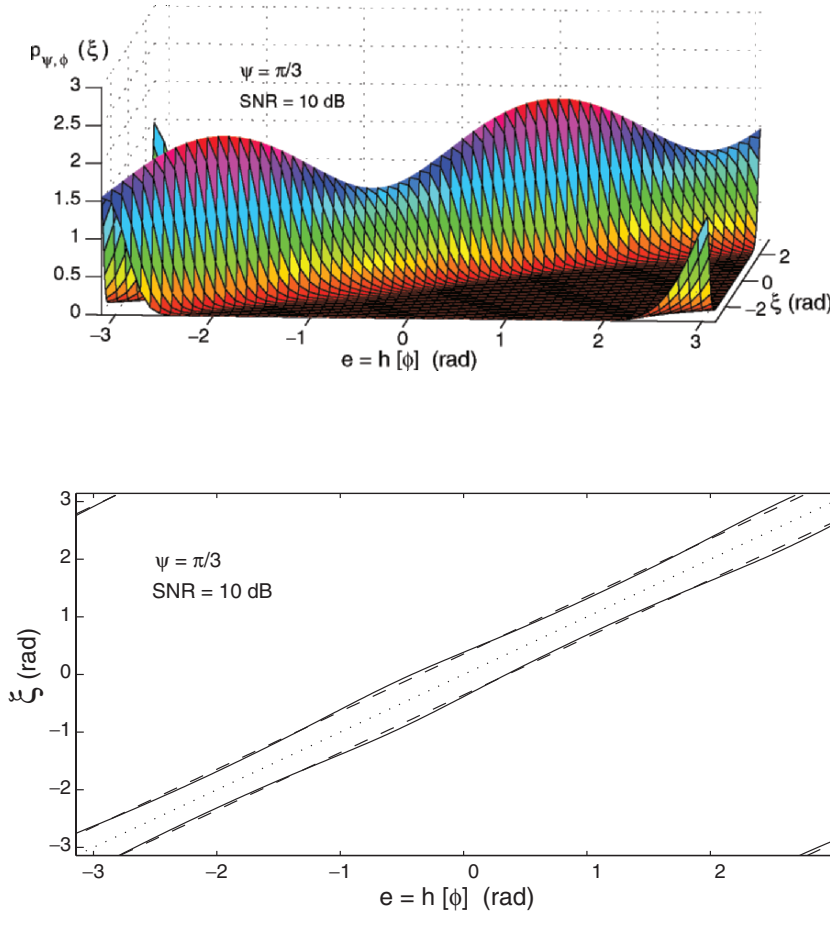


Figure 5.1: Above: the probability density function of the phase random variable ξ at the output of the phase error detector (PED) of TDTL, $p_{\psi,\phi}(\xi)$, for $\psi = \pi/3$ and SNR = 10 dB. Note that ϕ and $e = h[\phi]$ are the deterministic phase errors at the input and the output of the PED, respectively. Below: contour plot of the above $p_{\psi,\phi}(\xi)$ at the level of 0.5 for one period in the (e, ξ) plane (solid line) as compared to the that of CDTL (dashed line). Dotted line is the $\xi = e$ line. As SNR increases, the solid contour plot becomes two parallel lines as in the CDTL case.

as ψ approaches $\pi/2$. Note that this comparison is built on considering an ideal Hilbert transformer in CDTL, without taking into account the approximations and other practical problems associated with the implementation of the Hilbert transformer that are definitely reflected on the performance of the practical CDTL.

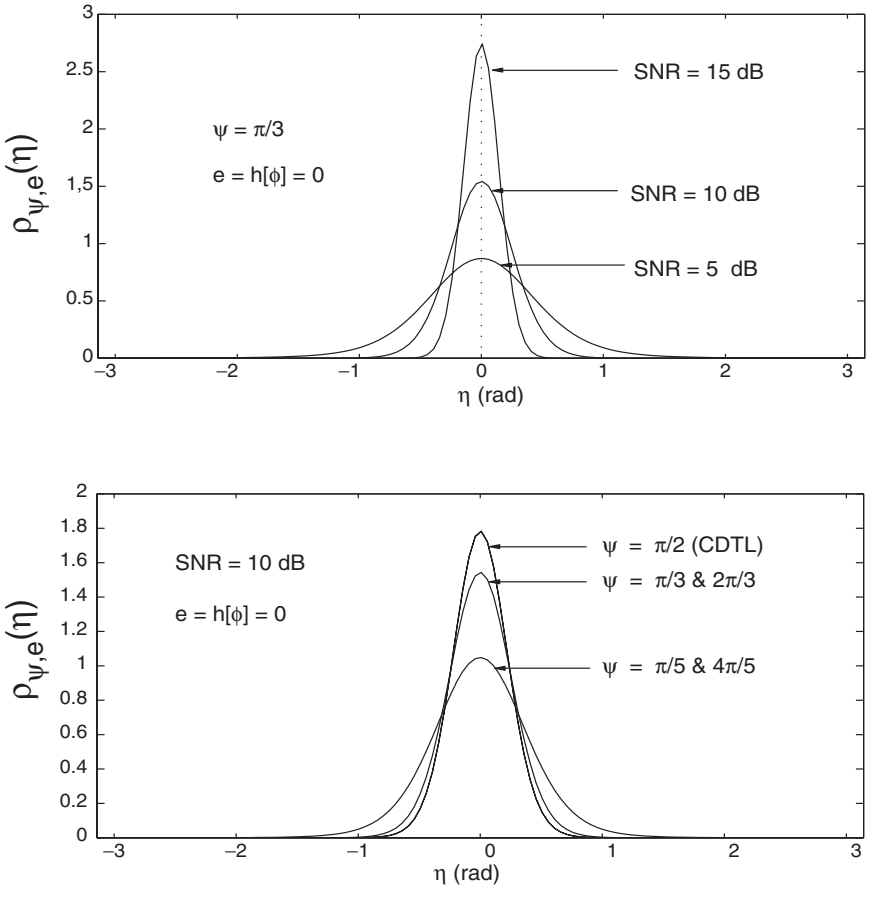


Figure 5.2: The probability density function $\rho_{\psi,e}(\eta)$ of the phase noise η at the output of the phase error detector (PED) of TDTL when $e = h[\phi] = 0$. Above: $\rho_{\psi,e}(\eta)$ for $\psi = \pi/3$ and different values of SNR. Below: $\rho_{\psi,e}(\eta)$ for SNR = 10 dB and different values of ψ. The expected value of η is always zero, but the variance is dependent on ψ and e. Similarity between curves is due to the ψ symmetry of $\rho_{\psi,e}(\eta)$.

5.2.4 Statistical Behavior of the TDTL in Gaussian Noise

In this subsection we study the steady-state pdf, expectation and variance of the modulo (2π) phase error at the input and the output of the phase error detector (PED) for the first and second-order TDTLs.

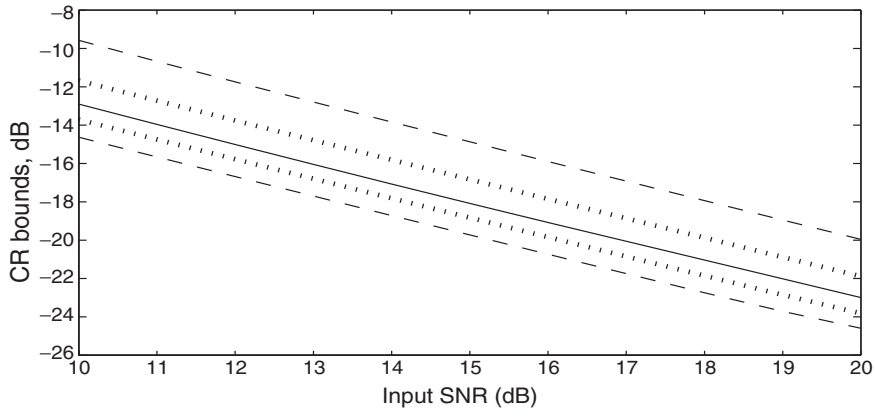


Figure 5.3: Ranges of the Cramer-Rao bounds of the phase estimator ξ at the output of the phase error detector of TDTL for $\psi = \pi/3$ & $2\pi/3$ (the area between dashed lines), and $\psi = 3\pi/7$ & $4\pi/7$ (the area between dotted lines). The range is found numerically for each ψ by calculating the CR bounds for the two extreme values of $m_{\psi,e}$ in the principal interval $-\pi < e \leq \pi$. Similarity in the CR bounds between ψ and $\pi - \psi$ is due to the ψ symmetry of the phase pdf. The solid line represents the CR bound of the (ideal) CDTL phase estimator, which is independent of the output phase true value e. As ψ approaches $\pi/2$, the range of the CR bounds approaches the CDTL case.

A. First-Order TDTL

(i) *Steady-State PDFs of the PED Input and Output Phase Errors*:

Since the two noise processes $\{n(k)\}$ and $\{n^{'}(k)\}$ discussed in Subsection (5.2.1) are independent, it follows that there effect on the phase would result in noise samples $\{\eta(k)\}$ that are independent for different sampling instants k.

The system equation of the first-order TDTL in the presence of noise can be obtained from (3.16) and (5.27) as follows

$$\phi(k+1) = \phi(k) - K_1^{'} h_\psi[\phi(k)] + \Lambda_o - K_1^{'}\eta(k) \tag{5.32}$$

where $\phi(k)$ is the phase error at the input of the phase error detector (PED) and $h_\psi(\phi(k)) = e(k)$ is the phase error at the output of the PED. Following the same analysis as in [13] and [43] we reach at the following Chapman-Kolmogorov

iterative equation

$$p_{\psi,k+1}(\phi|\phi_o) = \int_{-\infty}^{\infty} q_{\psi,k}(\phi|u)p_{\psi,k}(u|\phi_o)du \tag{5.33}$$

where $\phi_o = \phi(0)$, $p_{\psi,k}(\phi|\phi_o)$ is the pdf of $\phi(k+1)$ given ϕ_o, and $q_k(\phi|u)$ is the pdf of $\phi(k+1)$ given $\phi(k) = u$, which can be given in the case of TDTL by

$$\begin{aligned} q_{\psi,k}(\phi|u) &= \frac{1}{2\pi K_1'} \exp(-\mu_{\psi,u}\alpha) \\ &+ \frac{1}{K_1'}\sqrt{\frac{\mu_{\psi,u}\alpha}{\pi}}\cos\left(\frac{\phi-\nu}{K_1'}\right) \exp\left\{-\mu_{\psi,u}\alpha \sin^2\left(\frac{\phi-\nu}{K_1'}\right)\right\} \\ &\times \left(\frac{1}{2} + \operatorname{erf}\left\{\sqrt{2\mu_{\psi,u}\alpha}\cos\left(\frac{\phi-\nu}{K_1'}\right)\right\}\right) \end{aligned} \tag{5.34}$$

where $\nu = u - K_1' h_\psi[u] + \Lambda_o$ and the range of ϕ is the interval $(u+\Lambda_o - K_1'\pi, u + \Lambda_o + K_1'\pi)$.

The above iteration can be solved numerically by the Weinberg-Liu method explained in [13] and [43] to get the pdf of the steady-state phase error at the input of the PED, $\mathbf{p}_\psi(\phi)$.

The steady-state pdf of the phase error at the output of the PED, $\mathbb{P}(e)$ can be given by

$$\mathbb{P}_\psi(e) = \mathbf{p}_\psi\big(h_\psi^{-1}(e)\big)\,|d\phi/de| \tag{5.35}$$

where $e = h_\psi(\phi)$. From the above analysis we can deduce that the steady-state input and output phase error pdfs, $\mathbf{p}_\psi(\phi)$ and $\mathbb{P}_\psi(e)$, are dependent on $\Lambda_o = 2\pi(1-W)/W$, $\psi = \psi_o/W$, $K_1' = K_1/W$, and SNR. The CDTL phase error pdf was dependent on Λ_o, K_1', and SNR only [13].

(ii) *Steady-State Expectation of the PED Input and Output Phase Errors*:

In the steady-state we have $\mathcal{E}(\phi(k+1)) = \mathcal{E}(\phi(k))$ at the input of the phase error detector (PED). Also we have $\mathcal{E}(e(k+1)) = \mathcal{E}(e(k))$ at the PED output. It is worth noting that the steady-state phase errors ϕ_{ss} and e_{ss} are random variables in the presence of noise. Taking the expectation $\mathcal{E}$ of both sides of (5.32) under steady-state condition and solving for $\mathcal{E}(\phi_{ss})$ we have

$$\mathcal{E}(e_{ss}) = \mathcal{E}(h_\psi[\phi_{ss}]) = \{\Lambda_o - K_1'\mathcal{E}(\eta)\}/K_1' \tag{5.36}$$

where e_{ss} is the steady-state output of the PED. Since $\rho_{\psi,\phi}(\eta)$ is symmetric about zero, we have $\mathcal{E}(\eta) = 0$, hence we obtain

$$\mathcal{E}(e_{ss}) = \Lambda_o/K_1' \tag{5.37}$$

which is the same as the noise-free expression of e_{ss} given by (3.33). No additional condition in the presence of noise is implied by the above equation on $\lambda = \Lambda_o/K_1^{'}$. Hence only the noise-free condition on λ [given in (3.21)] is effective.

It is not straightforward to prove that the expectation functional $\mathcal{E}$ and the function h_ψ can be interchanged. However, according to the TDTL structure, a steady-state condition at the input of the PED implies a steady-state condition at the output of the PED. Therefore, the steady-state phase error at the output of the PED, $\mathcal{E}(e_{ss})$, should be in the following form

$$\mathcal{E}(e_{ss}) = h_\psi[\mathcal{E}(\phi_{ss})] \tag{5.38}$$

Using (3.14), (5.37), and (5.38) we obtain the following expression for $\mathcal{E}(\phi_{ss})$ by manipulations similar to those used in obtaining ϕ_{ss} in Section (3.3.1-C)

$$\mathcal{E}(\phi_{ss}) = \begin{cases} \alpha & \beta \ \sin(\lambda) \geq 0 \\ f\,[\alpha + \pi] & \text{otherwise.} \end{cases} \tag{5.39}$$

where $\lambda = \Lambda_o/K_1^{'}$, α and β are defined in (3.23) and (3.25). This is the same as the noise-free expression of ϕ_{ss} given by (3.33).

Hence in additive Gaussian noise, the first-order TDTL does not lose tracking of the input phase since the expected value of the phase error equals its deterministic value.

(iii) *Steady-State Variance of the PED Input and Output Phase Errors*:

Unlike CDTL, the variance of the steady-state input and output phase errors, ϕ_{ss} and e_{ss}, cannot be given in closed-form expressions in terms of $\mathcal{E}(\eta^2)$ and $K_1^{'}$. However, it can be obtained numerically from the steady-state pdfs $\mathbf{p}_\psi(\phi)$ and $\mathbb{P}_\psi(e)$ obtained in Subsection (5.2.4 - A (i)) above. For all values of ψ, the input variance and the output variance are decreasing functions of SNR. They are functions of ψ, $K_1^{'}$, and SNR. Numerical calculations have shown that, as in the case of CDTL, Λ_o only affects the expectation and has no effect on the variance. Also numerical calculations have shown that, for any ψ and SNR, the variance of the steady-state input and output phase errors is always positive inside the noise-free range of the effective parameters Λ_o and $K_1^{'}$. Hence no additional conditions are implied by the variance of the phase errors in the presence of noise.

Figure 5.4 shows the variance of the steady-state phase error at the output of the PED, $\text{var}(e_{ss})$, of the first-order TDTL with $\psi = \pi/3$ and $\psi = 2\pi/5$ as compared to that of CDTL for the same parameters $\Lambda_o = 0$ and $K_1^{'} = 0.7$ and 1. As ψ approaches $\pi/2$, TDTL variance approaches that of CDTL. Both CDTL

and TDTL has $\mathcal{E}(e_{ss})$ exactly at the noise-free value of e_{ss}, which is $\Lambda_o/K_1^{'}$, for all values of the parameters ψ, Λ_o and $K_1^{'}$. Note that the curves related to $\psi = 2\pi/3$ and $\psi = 3\pi/5$ are the same as the curves related to $\psi = \pi/3$ and $\psi = 2\pi/5$, respectively, due to the ψ symmetry of the phase pdf as given in (5.30).

B. Second-Order TDTL

We now discuss briefly the behavior of the second-order TDTL in noise since it can be obtained by analysis similar to that of the first-order TDTL discussed earlier.

In the presence of noise the system equation of the second-order TDTL can be obtained using (3.13), (3.35), and (5.27) as follows

$$\begin{aligned}\phi(k+2) &= 2\phi(k+1) - \phi(k) - rK_1^{'}\{h[\phi(k+1)] + \eta(k+1)\} \\ &\quad + K_1^{'}\{h[\phi(k)] + \eta(k)\} \qquad (5.40)\end{aligned}$$

Applying analysis similar to that in Subsection (5.2.4-A) above, we can obtain the steady-state pdf of the phase error at the input and the output of the phase error detector (PED). Taking the steady-state expectation of both sides of the above equation and noting that $\mathcal{E}(\eta) = 0$ at any sampling instant k, we obtain the expected value of the phase error at the output of the PED as follows

$$\mathcal{E}(e_{ss}) = 0 \qquad (5.41)$$

which is the same as the noise-free value of e_{ss}. By a reasoning similar to that in the previous Subsection, we obtain the expected value of the phase error at the input of the PED as follows

$$\mathcal{E}(\phi_{ss}) = 0 \qquad (5.42)$$

which is also the same as the noise-free value of ϕ_{ss}. As in the case of the first-order TDTL, the variance of the steady-state phase errors ϕ_{ss} and e_{ss} can be obtained numerically. It is now dependent on ψ, $K_1^{'}$, r, and SNR. Numerical calculations have shown that the variance is not affected by Λ_o and decreases as SNR increases or $K_1^{'}$ decreases. Also it decreases as r decreases. The variance is positive for all values of the parameters in the noise-free locking range, hence no additional conditions are implied on the second-order TDTL in the presence of Gaussian noise.

5.3 Conclusions

In this chapter we have analyzed the performance of the time-delay digital tanlock loop (TDTL) in the presence of additive Gaussian noise. The conventional

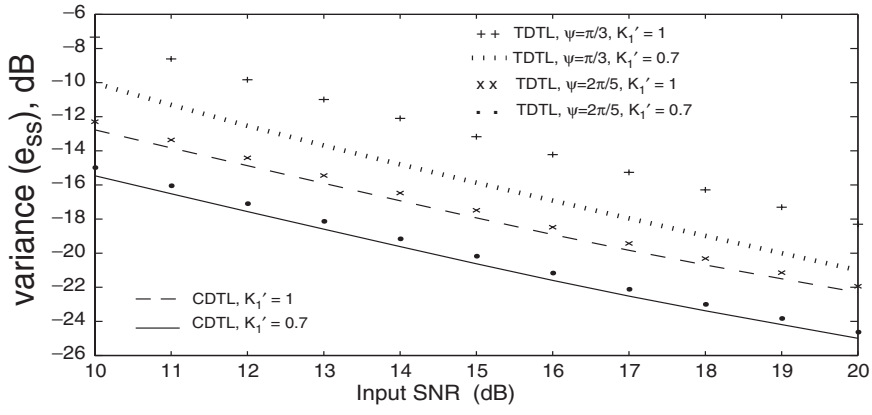


Figure 5.4: Variance of the steady-state phase error, e_{ss}, at the output of the phase error detector of the first-order TDTL with $\psi = \pi/3$ and $\psi = 2\pi/5$ as compared to that of CDTL for the same parameters $\Lambda_o = 0$ and $K_1^{'} = 0.7$ and 1. Note that Λ_o decides the expected value of e_{ss} and has no effect on the variance. As ψ approaches $\pi/2$, TDTL variance approaches that of CDTL. Both CDTL and TDTL has $\mathcal{E}(e_{ss})$ exactly at the noise-free value of e_{ss}, which is $\Lambda_o/K_1^{'}$. Note that the curves related to $\psi = 2\pi/3$ and $\psi = 3\pi/5$ are the same as the curves related to $\psi = \pi/3$ and $\psi = 2\pi/5$, respectively, due to the ψ symmetry of the phase pdf.

digital tanlock loop (CDTL) introduced significant advantages over other sinusoidal DPLLs, except for the complexity of the loop, and TDTL has the same merits with a reduced complexity. We have shown in Chapter 3 that although TDTL has a reduced structure as compared to the CDTL, it has a performance comparable to that of CDTL under noise-free conditions. In this chapter we have shown that the performance of TDTL in the presence of additive Gaussian noise is also successful and comparable to that of CDTL, especially under careful choice of the circuit parameters. Under the steady-state condition of operation, the first and second-order TDTLs have expected values of the phase error at the input and the output of the phase error detector (PED) exactly the same as their noise-free values, while the variance of the phase error is a decreasing function of the signal-to-noise ratio (SNR) and the loop parameter $K_1^{'}$ (in addition to r for the second-order TDTL). The variance also decreases and approaches CDTL case as the phase shift ψ (introduced by the time-delay) approaches $\pi/2$ from both sides. Hence TDTL does not lose tracking of the input phase in additive Gaussian noise in all cases. However, it is better in TDTL design to

choose a time-delay τ that gives a phase shift $\psi = \omega\tau$ as near to $\pi/2$ as possible during the expected range of the input frequency ω. No change in TDTL locking ranges is implied by the presence of Gaussian noise.

Chapter 6

Architectures for Improved Performance

6.1 Introduction

This chapter presents the simulation results of the conventional first-order and second-order TDTLs. The simulations show the behavior of both loops as they get subjected to various frequency disturbances. It also shows a variety of modified first-order TDTL architectures that are designed to enhance the performance of the conventional loop. The performance of the modified architectures is compared with that of the conventional first-order loop through a study of the transient responses and phase plane plots as the loops get subjected to large frequency steps. Similarly, modified second-order architectures are discussed and their performance is compared with the conventional second-order TDTL. Finally a variable order TDTL architecture that combines the desirable features of the first-order and the second-order is presented and its behavior is studied through simulation.

6.2 Simulation Results of First-Order TDTL

The first-order loop was tested by subjecting it to negative as well as positive input frequency steps. A negative step results in an input signal with frequency lower than that of the free running DCO, while a positive step has the opposite effect. An example of a negative frequency step is shown in Figure 6.1. In this case, the time delay and free running frequency of the DCO have been arranged so that the initial phase lag parameter $\psi_o = \omega_o\tau = \pi/2$, and the gain has been chosen as $K_1 = G_1\omega_o = 1.5$. When an input with a frequency ratio $W = \omega_o/\omega_i = 1.6$ is applied to the loop (i.e., an input frequency which is 1.6

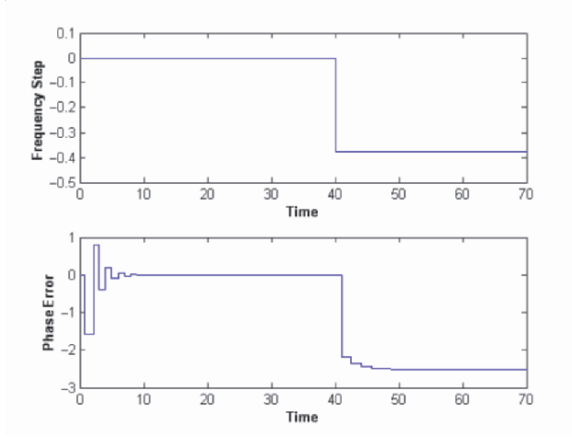


Figure 6.1: Top: Negative step input. Bottom: Loop response to the negative frequency step.

times less than the free running frequency), the loop converges to a steady-state of phase error since the input is within its locking range. This scenario is demonstrated in Figure 6.1.

Initially, an input of the same frequency as ω_o is applied, and it is clear that the phase error converges to zero before the negative frequency step occurs as shown in the bottom graph in Figure 6.1. Once the frequency change is applied, the phase error assumes a negative value owing to the fact that the input is of a less frequency. The TDTL then converges to a steady state phase error, i.e., the loop is in a lock-state and the DCO is tracking the input frequency. The convergence to a non-zero steady state phase error is a unique property of the first order loop. This is caused by the proportional filter, which is incapable of providing sufficient error signal to drive the phase error to zero.

The sampling process of the DCO is shown in Figure 6.2, where it is clear that the DCO locks to positive-going zero crossing before applying the frequency step, and varies its period until it matches the new input frequency after the frequency change is applied. The effect of converging to a non-zero phase error is evident from the phase offset positive-going zero crossings and the DCO pulses.

The first-order loop has also been tested for positive frequency steps, i.e., for input signals with frequency higher than ω_o, and an example is shown in

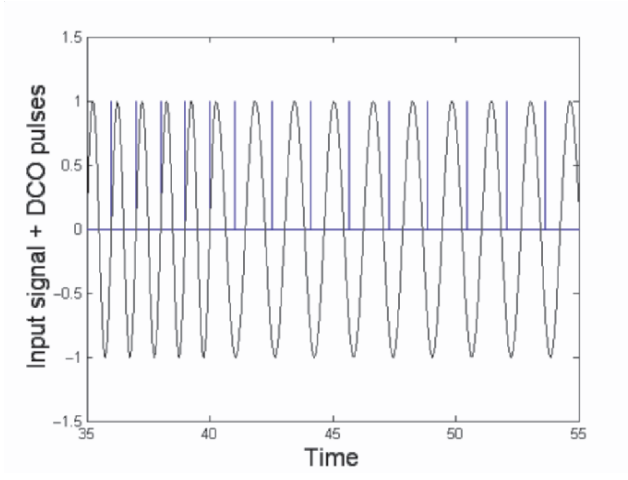


Figure 6.2: Sampling process of the first-order TDTL (negative step).

Figure 6.3. The time delay τ and the free running frequency ω_o have been arranged such that $\psi_o = \pi/3$, and the gain has been chosen as $K_1 = G_1\omega_o = 1.3$. A frequency step with $W = \omega_o/\omega_i = 0.5$ (i.e., twice ω_o) is applied to the loop, and as shown in Figure 6.3, the phase error reaches a positive steady state value indicating that the loop is in-lock with the input frequency.

The above results demonstrate that the TDTL has fast acquisition as it is capable of locking to an input signal within a few samples. It also has a wide locking range which enables it to deal with large frequency steps as show in Figures 6.1 and 6.3 above. However, due to the nonlinear characteristics of the TDTL optimality cannot be achieved in terms of the loop parameters. In other words, the advantageous performance characteristics, such as the fast acquisition and the wide locking range, are dependent on a set of parameters such as the loop gain K_1 and the nominal phase lag ψ_o. Tuning these parameters however, is based on trial and error and there is always a trade-off between the wide locking range and the fast acquisition characteristics [82]. The next section presents different modifications of the loop that enable the control of the loop gain and phase lag and hence improve its performance.

The nonzero steady state phase error of the first order TDTL, as shown in Figures 6.1 and 6.3, is due to the loop filter which is only a gain block in this

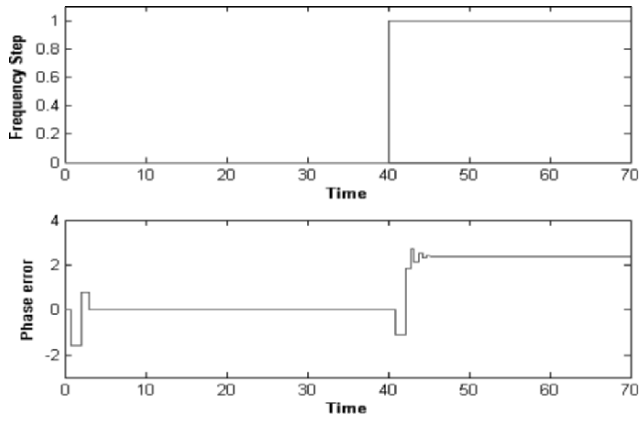


Figure 6.3: Top: Positive step input. Bottom: Loop response to the positive frequency step.

case. This disadvantage can be eliminated by increasing the order of the loop to second order. However, this will be at the expense of a reduction in the loop locking range. Therefore, depending on the application in which the loop is to be used the appropriate order of the loop should be selected. For example, the nonzero steady state phase error of the first order TDTL would indicates the existence of a phase offset between the input and the recovered carrier, hence violating the conditions of coherent demodulation [3, 80] and effectively precluding its use in such applications.

6.3 Improved First-Order TDTL Architectures

This section discusses modified first-order TDTL architectures that overcome some of the loop limitations and improve it's performance in terms of speed and locking range width. These modifications are based on the use of finite-state machines to control particular loop parameters and hence achieve the desired performance. The proposed architectures and their associated simulation results are described in the subsections below.

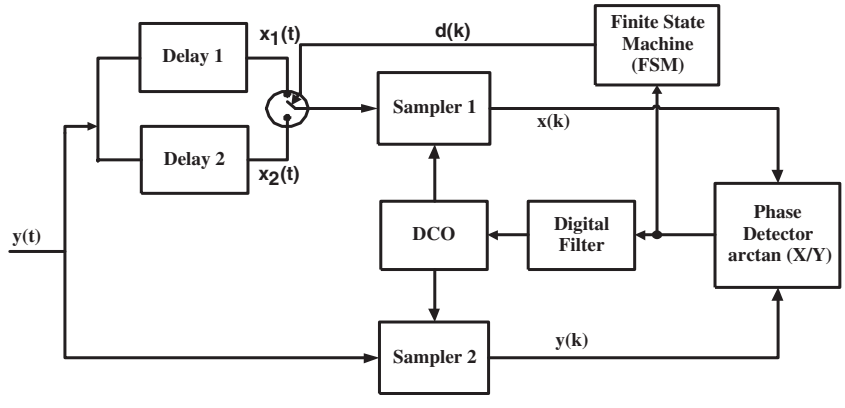


Figure 6.4: Variable delay TDTL architecture.

6.3.1 Delay Switching Architecture

Since the value of the time delay is of great influence on the convergence behavior of the loop. The conflicting requirements of fast acquisition and wide locking range necessitate the inclusion of more than one time delay [82, 83]. The structure of the variable delay TDTL (VD-TDTL) is shown in Figure 6.4. It is clear that it resembles the TDTL discussed earlier; however, the time delay unit has been exchanged with a dual delay structure, which is controlled by a finite state machine (FSM) block. The time delay units generate two phase shifted versions of the input signal, which are given by

$$x_1(t) = A\sin\left[\omega_o t + \theta(t) - \psi_1\right] \tag{6.1}$$

$$x_2(t) = A\sin\left[\omega_o t + \theta(t) - \psi_2\right] \tag{6.2}$$

The control signal $d(k)$, which is the output of the FSM, decides which of the signals given in (6.1) and (6.2) are to be passed to Sampler 1 in order to produce the following discrete time signal

$$x(k) = A\sin\left[\omega_o t(k) + \theta(k) - \psi_i\right] \tag{6.3}$$

where i is a subscript indicating the time delay block. The signal in (6.3) can be redefined in terms of the phase error as

$$x(k) = A\sin\left[\phi(k)\right] \tag{6.4}$$

and therefore, the error signal can be re-written as

$$e(k) = f\left[\mathrm{Tan}^{-1}\left(\frac{\sin\left[\phi(k)\right]}{\sin\left[\phi(k)+\psi_i\right]}\right)\right] \tag{6.5}$$

where Tan^{-1} is the 4-quad arctan. Since the proposed variable delay TDTL is implemented as a first-order loop, the system difference equation will be the same as that given in (3.16), and consequently the locking range can be found by solving the following inequality:

$$2\left|1-W\right| < K_1 < 2W\frac{\sin^2(\alpha)+\sin^2(\alpha+\psi_{oi})}{\sin(\psi_{oi})} \tag{6.6}$$

where ψ_{oi} is the nominal phase shift.

In the proposed system, the time-delay units have been arranged so that $\psi_{o1} = \pi/2$ and $\psi_{o2} = \pi/3$, which will produce the locking range curves shown in Figure 6.5. This will ensure a symmetric tracking range from $W = 0.5$ up to $W = 1.5$. Hence, the system will exploit the wide range and fast acquisition characteristics of ψ_{o1} in the area where $W > 1$, and of ψ_{o2} in the area where $W < 1$. The loop gain $K_1 = 1.13$ has been selected to ensure good performance and wide locking range for both values of the time-delay.

The states of the FSM are defined by the phase error and the control signal $d(k)$. If the system is subjected to a frequency step causing the input signal frequency to go higher than ω_o, i.e. $W < 1$, and the phase error is greater than a predefined threshold $\varepsilon_1 > 0$, the control signal $d(k)$ will allow the signal $x_2(t)$ to pass to Sampler 1. If the system is subjected to a frequency step which causes the input frequency to go lower than ω_o, i.e., $W > 1$, the FSM will monitor the phase error until it is below another threshold $\varepsilon_2 < 0$, then the control signal $d(k)$ will allow the signal $x_1(t)$ to pass to Sampler 1. The parameters ε_1 and ε_2 allow fine-tuning of the FSM behavior for any intended region of operation of the loop in order to ensure fast acquisition behavior.

Figure 6.6-a shows the transient response of the single delay loop with $\psi_{o1} = \pi/2$ and $K_1 = 1.13$ to a frequency step with $W = 0.5$. Since this mode of operation is outside the locking range of the loop, the phase error diverges to an unstable state, thus throwing the loop in the unlocked mode. This is also illustrated in Figure 6.6-b, which shows the phase plane plot for the same frequency step; where it is clear that the phase does not converge to a steady state value. The result of applying the same frequency step to the same TDTL but with ψ_{o2} is shown in Figure 6.7-a. It can be clearly seen that the phase error settles within a few samples. The same result can also be depicted by examining the phase plane plot of Figure 6.7-b, which indicates the convergence of the phase error.

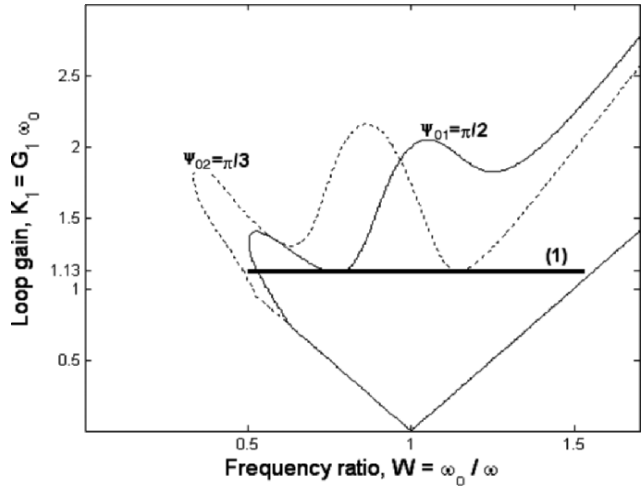
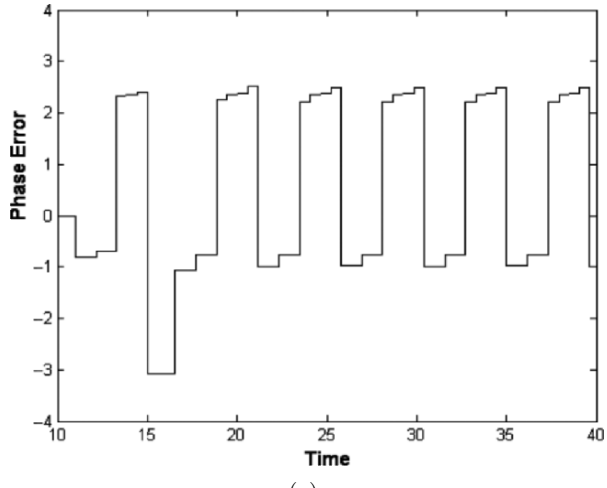
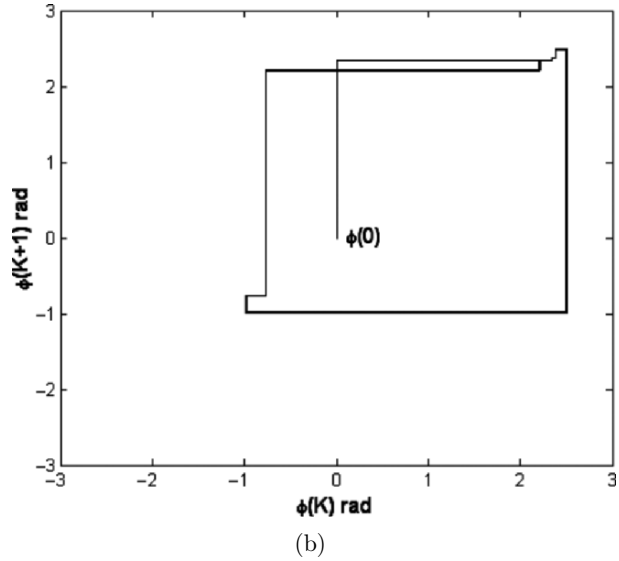


Figure 6.5: Locking range of first-order TDTL with different values of ψ_o, the tracking range is the bold line (1).

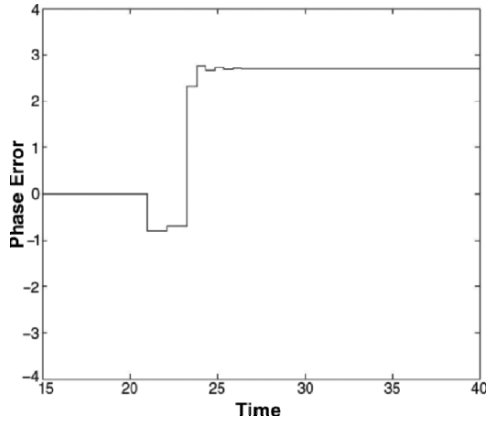


(a)

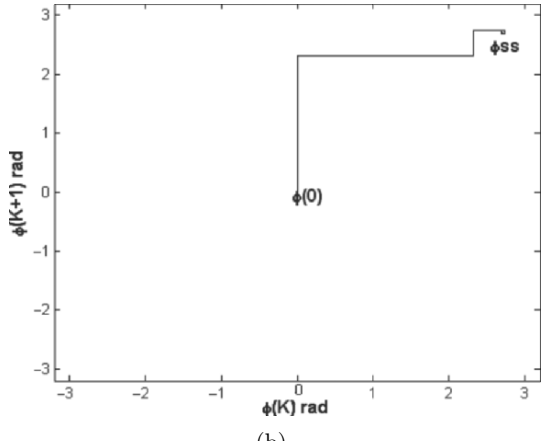


(b)

Figure 6.6: (a)Transient response of the single delay TDTL with $\psi_{o1} = \pi/2$ and $K_1 = 1.13$ to a frequency step with $W = 0.5$ (b) Phase plane behavior.



(a)



(b)

Figure 6.7: (a)Transient response of the single delay TDTL with $\psi_{o2} = \pi/3$ and $K_1 = 1.13$ to a frequency step with $W = 0.5$ (b) Phase plane behavior.

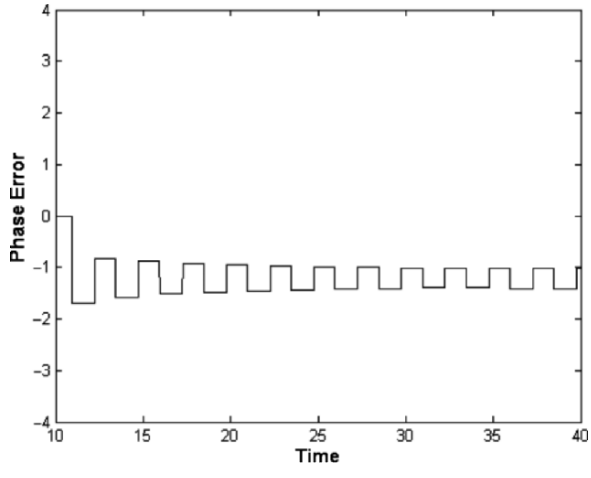


Figure 6.8: Transient response of the single delay TDTL with $\psi_{o2} = \pi/3$ and $K_1 = 1.13$ to a frequency step with $W = 1.25$.

Another scenario is illustrated in Figure 6.8 with a negative frequency step. It is clear that the transient response of the single delay TDTL with $\psi_{o2} = \pi/3$ and $K_1 = 1.13$ to a frequency step with $W = 1.25$ is poor as the phase error is not converging to a steady state value within an acceptable time. Whereas the transient response of the same TDTL with $\psi_{o2} = \pi/3$ for the same frequency step, demonstrated in Figure 6.9, shows that the phase error converges to a steady state value in two samples. The merit of using the VD-TDTL is that it is capable of distinguishing, in both of the aforementioned situations, the delay that yields the optimum performance. Thus, the previous graphs with steady-state phase error are corresponding to the response of the VD-TDTL under the same operating conditions.

6.3.2 Adaptive Gain Architecture

If the conventional TDTL is thrown out of lock due to a sudden change in the input frequency, it will stay out of lock unless an external signal forces the digitally controlled oscillator (DCO) back into the locking region. In order to ensure stable operation of the TDTL, it has to keep operating within the

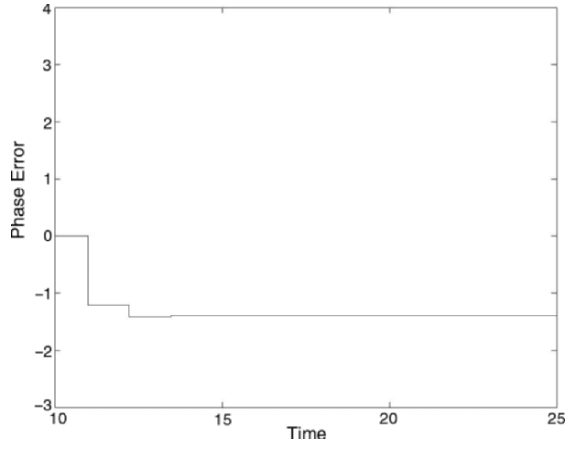


Figure 6.9: Transient response of the single delay TDTL with $\psi_{o1} = \pi/2$ and $K_1 = 1.13$ to a frequency step with $W = 1.25$.

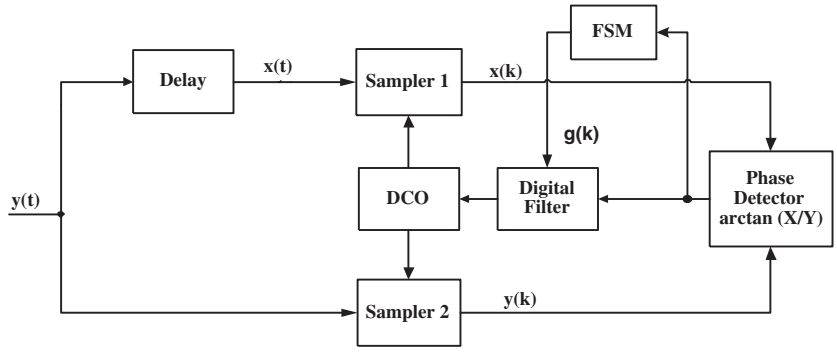


Figure 6.10: Structure of the adaptive gain TDTL.

locking boundaries, and this can be achieved by adapting the gain in response to out-of-range frequency signals [84]. The proposed architecture to achieve this is shown in Figure 6.10.

The adaptive TDTL in Figure 6.10 is created by utilizing a variable gain digital filter, which is controlled by means of an appropriate FSM. Choosing the nominal phase lag of the loop ψ_o to be equal to $\pi/2$ ensures the best state of linearity in the phase detector output. Thus, the phase error is approximately proportional to the radian frequency of the input, and can be used as an indicator of the operating point of the loop within the locking boundary shown in Figure 6.11. The scenario given below explains the operating principles of the adaptive gain TDTL.

Assuming that the first-order loop is initialized with a loop gain K_1 of 0.5, this has the advantage of reducing the TDTL performance degradation due to noise, since the variance of the phase error is a decreasing function of the loop gain K_1 and the signal to noise ratio [82]. The locking range boundary indicates that the loop can acquire the frequencies of all inputs bounded by the points A_1 and A_2 in Figure 6.11. However, it is very likely that the loop will be subjected to some disturbances or large frequency steps that will throw the system out of lock, e.g., the system will be thrown to point B or D. Normally, this will not be recovered by the conventional TDTL and the loop will carry on in the unlocked state.

However, the adaptive gain TDTL in Figure 6.10 senses, using the phase error, that the operating point has been moved outside the locking boundary,

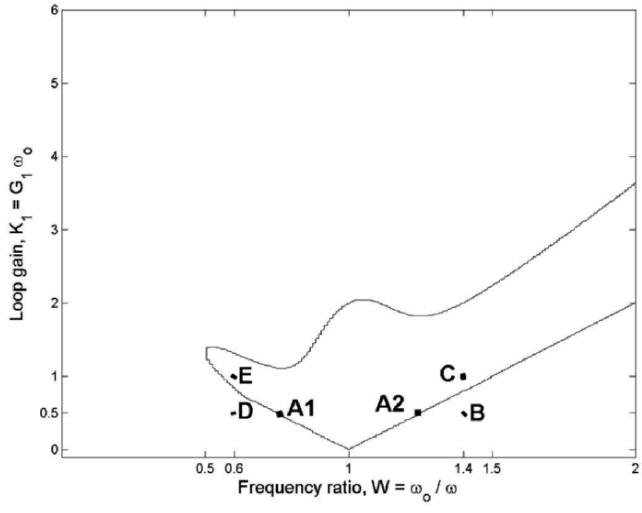
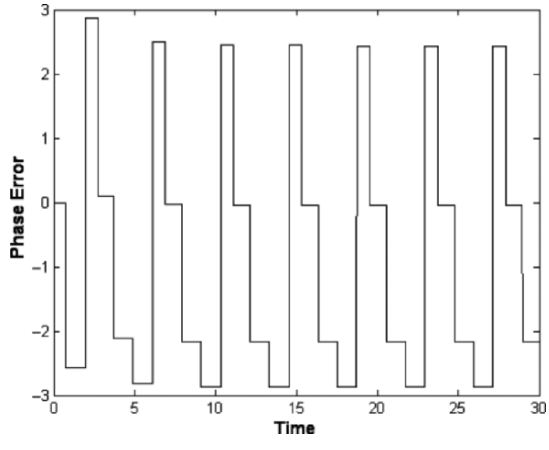


Figure 6.11: Locking boundary of the adaptive TDTL.

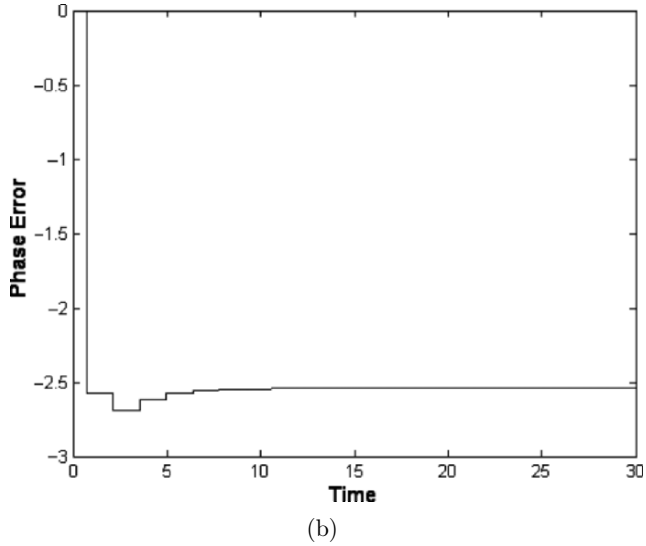
and therefore the FSM updates the gain of the digital filter, thereby moving to points C or E, which are inside the locking boundary of the system. The overall locking range of this implementation has been extended symmetrically from $W = 0.6$ to $W = 1.4$. The mathematical analysis of the adaptive gain TDTL is similar to that of the original TDTL discussed earlier.

The improved loop in Figure 6.10 was tested by subjecting it to large frequency steps (large phase errors) that force the system to go outside the nominal locking range, such as points B and D, in Figure 6.11. In both test cases the system senses the phase error through its FSM and accordingly adjusts the gain of the digital filter in such a way that out of lock operating points B and D are pulled to in lock points C and E respectively. The settling behavior of the loop at points B and C is shown in Figure 6.12. The locking behavior at the same points is also demonstrated by the phase plane plots in Figure 6.13. The plots show that when the loop is at point C it converges into a steady state condition within an acceptable number of samples, whereas when the loop is at point B it stays in the unlocked condition.

When the loop is subjected to a large step in frequency causing the system to go outside the locking range, e.g. point D in Figure 6.11, the system senses

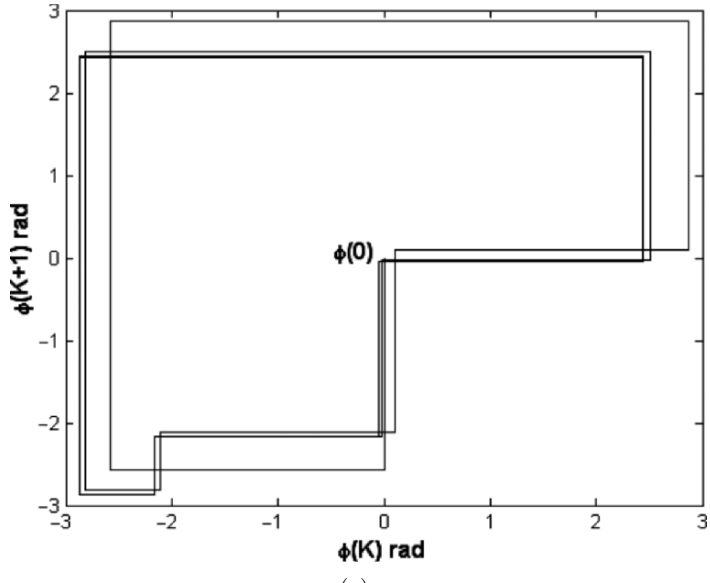


(a)

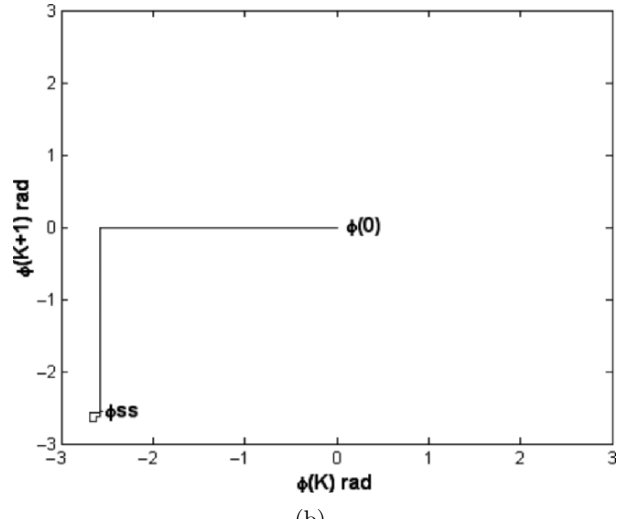


(b)

Figure 6.12: (a) Transient response of the system at point B. (b) Transient response of the system at point C.



(a)



(b)

Figure 6.13: (a) Phase plane of unsettled system at point B. (b) Phase plane of settled system at point C.

this error through the FSM and updates the gain of the digital filter to bring the operating point within the locking region at point E. The settling time of the loop at points D and E are shown in Figure 6.14, and the phase plots are illustrated for the same operating points in Figure 6.15.

6.3.3 Combined Delay Switching and Adaptive Gain

The previously mentioned methods of TDTL enhancement offer attractive aspects in terms of locking range and acquisition characteristics. However, the outcome of improvement can be increased by combing the two techniques into the TDTL, which yields a loop with faster acquisition, wider locking range and more resilience to frequency disturbances.

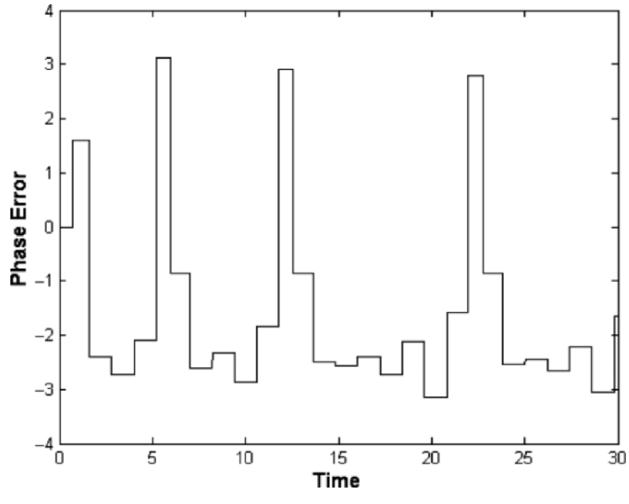
The proposed loop architecture is depicted in Figure 6.16, where as can be seen it is a combination of the two previously mentioned architectures [85]. However, the FSM is being fed by discrete time outputs of the samplers, namely $x(k)$ and $y(k)$. On the other hand, the gain of the digital filter and the active time delay unit is controlled by the $g(k)$ and $d(k)$ respectively, which are the output signals of the FSM.

Signals $x_1(k)$ and $x_2(k)$ are the same as those described by (6.1) and (6.2). Following the same analysis, the difference equation of the system is given by

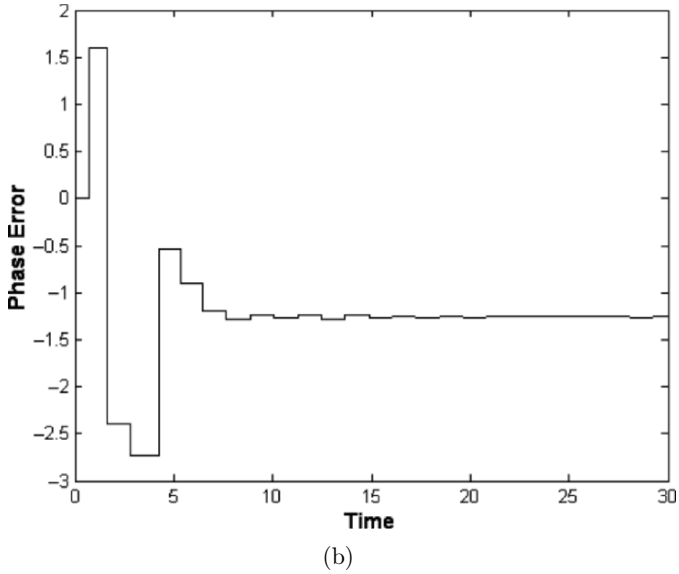
$$\phi(k+1) = \phi(k) - \omega G_s h\left[\phi(k)\right] + \Lambda_o \tag{6.7}$$

Where G_s denotes the variable gain of the digital filter, and s is a unique code corresponding to each state of the FSM. The locking range can be acquired by solving the inequality given by (6.6), resulting in a locking range which is similar to that of the conventional TDTL in Chapter 3. The operating point of the TDTL is defined in terms of the frequency ratio W, the nominal phase shift ψ_{oi} and the loop gain K_1. Since the two latter parameters are usually predefined, the changes in the operating point are dependent on an external parameter, which is the frequency of the input signal; this will move the operating point either inside or outside the locking boundary of the loop.

The resilience of the loop to frequency disturbances is increased in the adaptive gain and delay TDTL by introducing two extra degrees of freedom, namely the digital filter gain G_s and the nominal phase shift Ψ_{oi}. These will be tuned by the FSM to ensure that the loop operates within the locking range of the loop regardless of changes in the input frequency. The time delay units have been arranged so that $\psi_{o1} = \pi/2$ and $\psi_{o1} = \pi/3$, and areas of operation have been mapped to the states of the FSM, where each state will have a unique gain G_s and phase shift Ψ_{oi}. The system will switch between the delays according to the frequency of the input, so that ψ_{o1} operates in the area where $W > 1$,

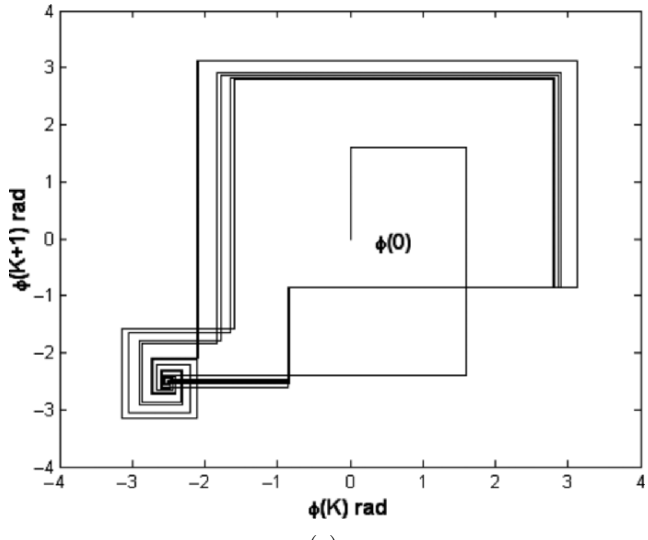


(a)

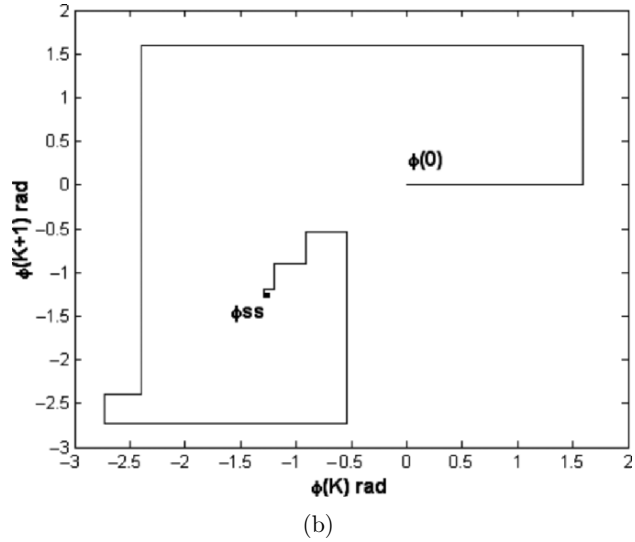


(b)

Figure 6.14: (a) Transient response of the system at point D. (b) Transient response of the system at point E.



(a)



(b)

Figure 6.15: (a) Transient response of the system at point D. (b) Transient response of the system at point E.

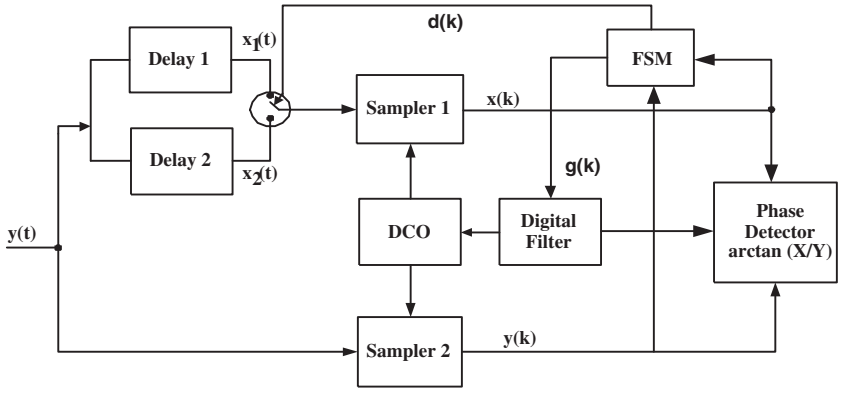


Figure 6.16: Adaptive gain and delay TDTL.

and ψ_{o2} operates in the area where $W < 1$, and this is mainly due to the wide range offered by each delay in its defined region of operation.

Therefore, the overall locking range of the proposed system will increase and a new locking boundary can be defined as shown in Figure 6.17, which also shows the tracking range of the system (the bold line inside the locking boundary). It encapsulates the different possibilities of loop operation points. It is clear that this range extends from $W = 0.4$ up to $W = 1.65$. The FSM ensures mapping each change of frequency to its desired operating point within the tracking range. Two main measures are provided by the FSM to counter the effect of frequency changes, the first is to set the active time delay, and the second is to make any necessary changes in the value of the digital filter gain. The FSM criteria for state transition is based on the signs of the signals $x(k)$ and $y(k)$, which provide meaningful information about the frequency of the input signal.

To illustrate the improvement in the system performance that the architecture in Figure 6.16 gives, a frequency step of $W = 0.4$ is applied to the original TDTL in Figure 3.1 with $\psi_{o1} = \pi/2$ and $K_1 = 1$. This drives the loop into the unlocked state, and the therefore the phase error will assume an unstable behavior as illustrated in Figure 6.18. When the same frequency input is applied to the adaptive gain and delay TDTL, it yields the transient response illustrated in Figure 6.19-a. As the figure shows, the phase error oscillates during the first two samples, indicating an out-of-range frequency, however, the FSM then forces the system back into the locked state, which is clearly shown as

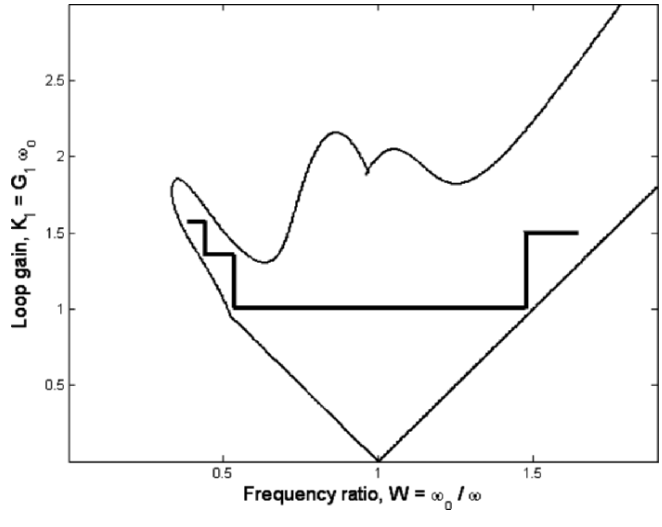


Figure 6.17: Unified locking range of the adaptive gain and delay TDTL.

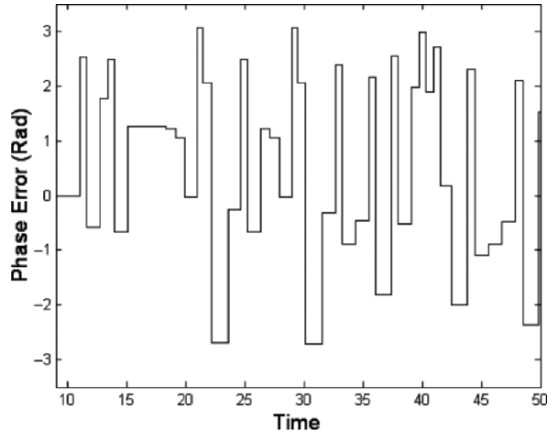


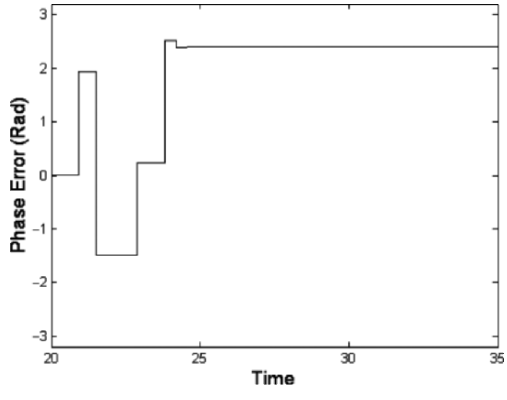
Figure 6.18: Transient response of the single delay TDTL with $\psi_{o1} = \pi/2$ and $K_1 = 1$ to a frequency step with $W = 0.4$.

the phase error converges to a steady state value afterwards. The phase plane portrait shown in Figure 6.19-b also supports this result.

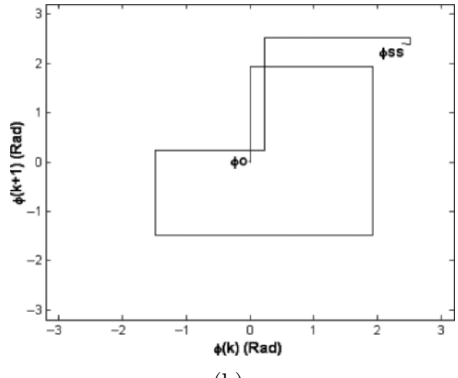
Another test case is conducted at the low frequency part. Figure 6.20-a demonstrates the transient response due to a frequency step of $W = 1.65$, where the loop responds rapidly and converges to a steady state phase error within five samples, two of which are consumed by the FSM to decide on the operating point. The phase plane portrait shown in Figure 6.20-b also demonstrates this result.

6.3.4 Sample Sensing Adaptive Architecture

Figure 6.21 shows an improved TDTL architecture that uses an error-sensing block to monitor the samples in the delayed path of the loop before they get fed to the arc-tan phase detector. The error-sensing block includes an FSM whose output $G(k)$ is used to control the gain of the digital filter. The appropriate adjustment of the filter gain ensures that the loop remains in lock when subjected to large frequency disturbances that would otherwise result in out of lock condition. The error-sensing block has a fast response, as it does not need to wait for the arc-tan phase detector to finish processing a sample. Overall the new loop offers enhanced performance compared with the original TDTL designs [105].

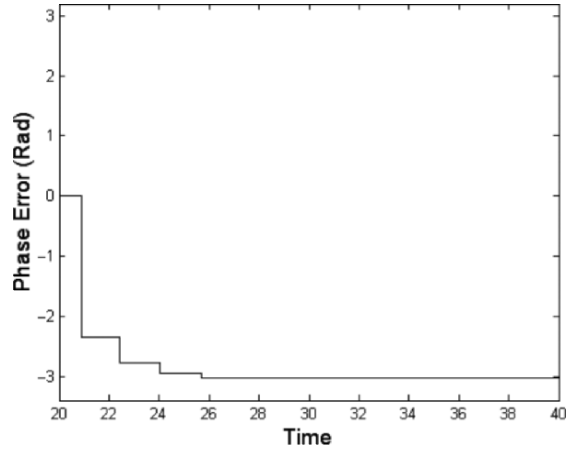


(a)

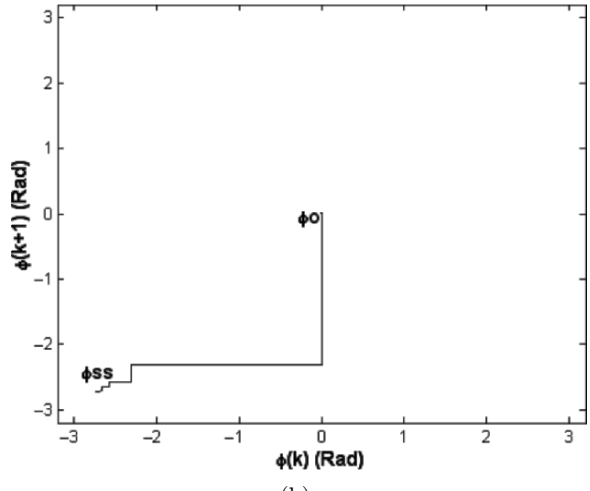


(b)

Figure 6.19: (a) Transient response, adaptive gain and delay TDTL response to a frequency step with $W = 0.4$. (b) Phase plane behavior.



(a)



(b)

Figure 6.20: (a) Adaptive gain and delay TDTL transient response to a frequency step with $W = 1.65$. (b) Phase plane behavior.

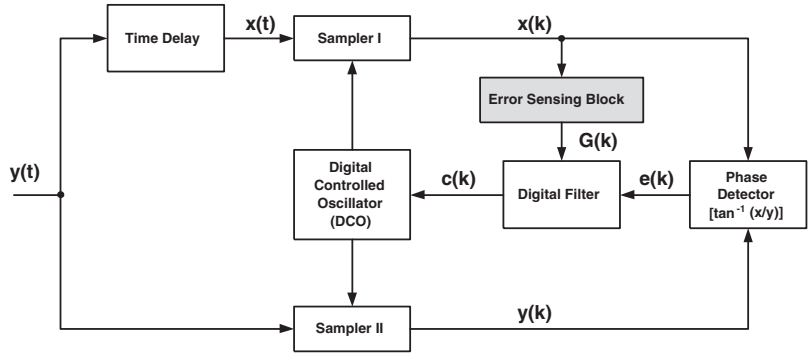


Figure 6.21: Sample sensing adaptive TDTL.

Figure 6.22 depicts the locking boundary of the sample sensing adaptive TDTL (SS-ATDTL) with $\psi_o = \pi/2$. In the original TDTL, if the system is thrown out of lock due to a sudden change in the input frequency it will stay out of lock unless an external signal forces the DCO back into the locking region. In the case of the system shown in Figure 6.21, the error-sensing block with its adaptive capabilities ensures that the loop stays in a locked state even if it is subjected to large phase errors. The behaviors of the SS-ATDTL and the original TDTL were studied assuming that the initial stable point of operation for each loop is point A in Figure 6.22, where $W = 1$ and $K_1 = 0.5$. This choice would result in a good signal to noise ratio for the overall system.

Subjecting the conventional TDTL to frequency disturbances that drive to say point C or D in Figure 6.22 will drive the system out of lock. However, subjecting the SS-ATDTL to the same disturbances will make the error sensing block generate an error signal that corresponds to a unique step value of the input frequency, consequently the FSM adjusts the digital filter gain to a new value G_s that forces the DCO to adjust to the new frequency before the system goes out of lock. The same process is followed for both positive and negative steps, that is for $W < 1$ and $W > 1$ respectively. For example, if the proposed system gets driven by a frequency step to point C in Figure 6.22 where $K_1 = 0.5$, it regains stability by increasing G_1 until $K_1 = 1$ and hence move the system to point B. Similarly, if the system is driven to point D it stabilizes by moving to point E. As can be seen in Figure 6.22, both points B and E are within the locking range of the loop.

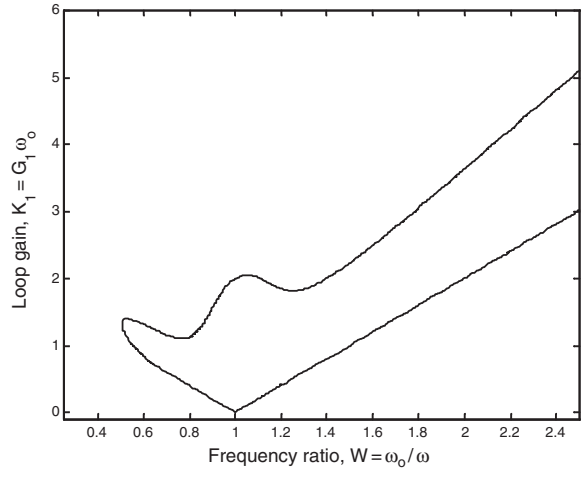
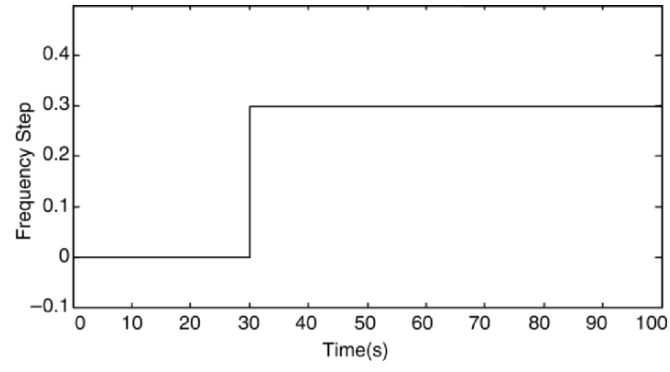


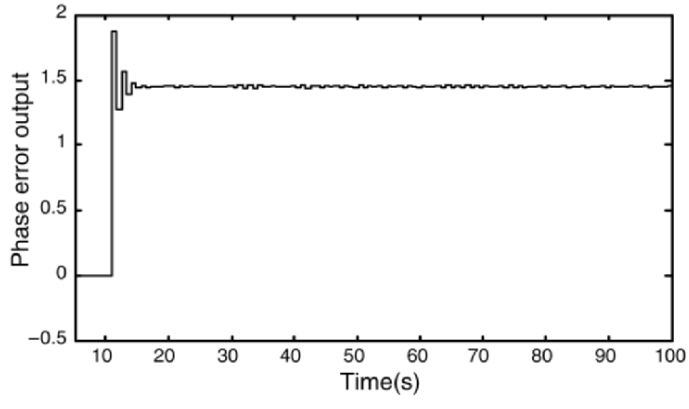
Figure 6.22: The locking range of the TDTL at $\psi_{o1} = \pi/2$.

An example of comparing the SS-ATDTL and the original TDTL responses to a positive frequency step is shown in Figure 6.23. In this test, the time delay and free running frequency of the DCO have been arranged so that $\psi_o = \pi/2$, and the gain of the TDTL has been chosen as $K_1 = 0.5$, and an input frequency step of 0.3 with $W = 0.769$. Initially the frequency of the input was equal to ω_o, therefore the phase error settled at zero. Then a positive frequency step was applied to the loop, causing the phase error to jump to a positive value indicating that the input frequency is higher than the loop frequency. The loop then locks to the new input frequency but with a phase shift settling at a constant positive value. Figure 6.23 shows that the SS-ATDTL locks to the input step faster than the conventional TDTL but with a bit larger steady state phase error value.

The phase plane plots in Figure 6.24 and the DCO sampling process shown in Figure 6.25 confirm the above results. The figures give an indication of the relative speed of locking. Figure 6.25 also shows the constant phase error in the two loops, which is due to the fact the both loops are of the first order type.



(a)



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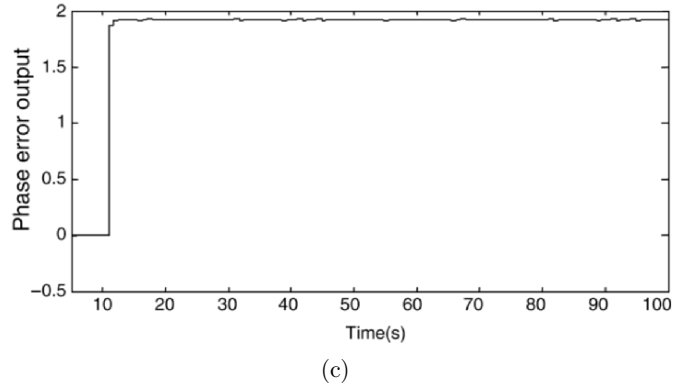
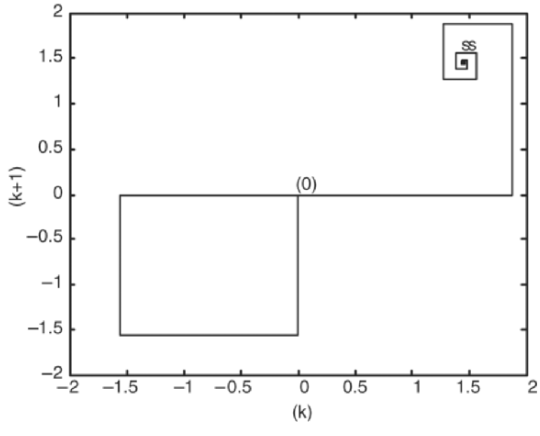
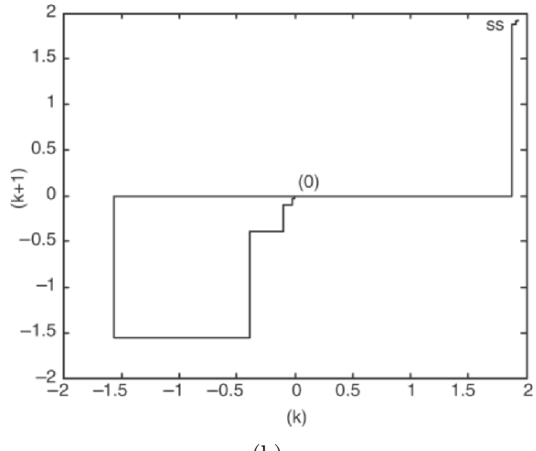


(c)

Figure 6.23: (a) Positive frequency step. (b) Original TDTL response. (c) SS-ATDTL response.

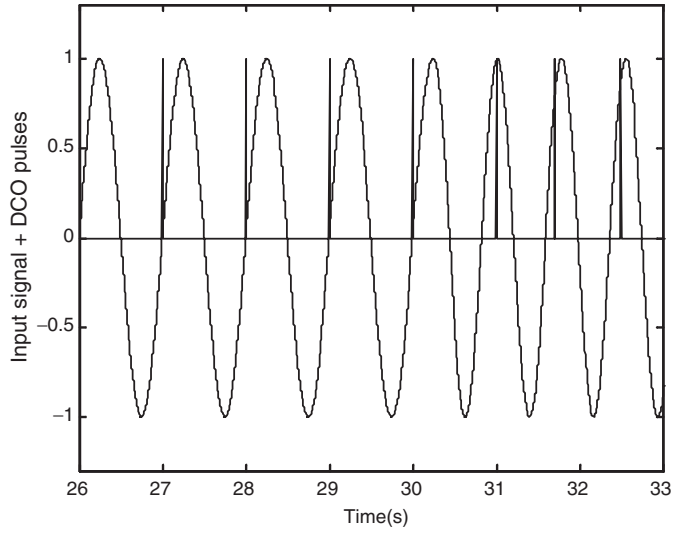


(a)

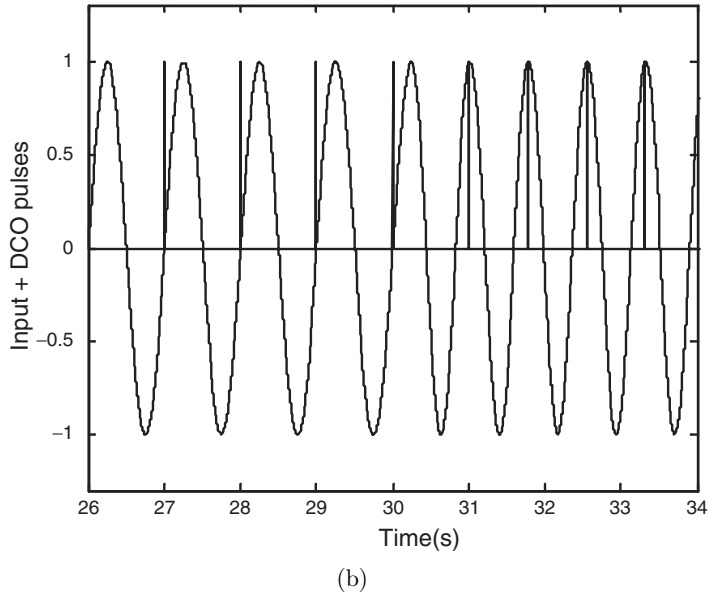


(b)

Figure 6.24: Phase plane plots: (a) Conventional TDTL (b) ATDTL.



(a)



(b)

Figure 6.25: DCO Sampling process of (a) original TDTL (b) SS-ATDTL.

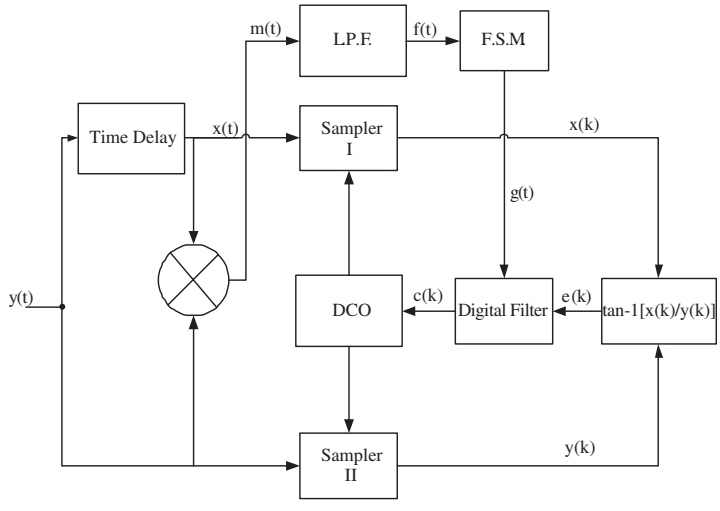


Figure 6.26: Early error sensing adaptive TDTL.

6.3.5 Early Error Sensing Adaptive Architecture

This section describes an early error sensing adaptive TDTL (EES-ATDTL) architecture. A block diagram of the EES-ATDTL is depicted in Figure 6.26. The architecture exploits the fact that the phase shift introduced by the time delay unit is directly proportional to the input frequency, this means that any frequency shift that occurs at the input can be detected by calculating the phase difference between the signals in the two arms of the TDTL [106], namely $y(t)$ and $x(t)$.

To find the phase difference, the error detector uses a multiplier followed by a low pass filter and an FSM. Under noise-free conditions, the loop accepts a sinusoidal input $y(t)$ having a radian frequency ω with a frequency offset $\Delta\omega = \omega - \omega_o$ from the nominal radian frequency ω_o of the DCO. The input signal is given by

$$y(t) = A\sin[\omega_o t + \theta(t)] \tag{6.8}$$

Where A is the signal amplitude and $\theta(t)$ is the phase of the incoming signal. Assuming a frequency step at the input then

$$\theta(t) = (\omega - \omega_o)t + \theta_o \tag{6.9}$$

where ω is the radian frequency of the input signal and θ_o is a constant. The time delay unit introduces a constant time-delay τ in the input signal, which causes a phase lag $\psi = \omega t$. Therefore, the time-delayed signal can be expressed as

$$x(t) = A\sin[\omega_o t + \theta(t) - \psi] \tag{6.10}$$

and the output of the multiplier is

$$\begin{aligned} m(t) = x(t) \cdot y(t) &= A^2 \sin[\omega_o t + \theta(t) - \psi] \cdot \sin[\omega_o t + \theta(t)] \\ &= (A^2/2)[\cos(\psi) - \cos(2\omega_0 t + 2\theta(t) - \psi)] \end{aligned} \tag{6.11}$$

Equation (6.11) shows that the output of the multiplier consists of two parts, the first one is a function of only the phase difference of the two signals, and the second term is at a frequency that is twice the signal frequency plus the sum of the two phases.

In Figure 6.26 the low pass filter bandwidth is quite small so that it both filters out the noise and the unwanted double frequency term. If initially no frequency shift is applied to the input then the phase difference will be zero (actually $\psi_o = \pi/2$) and consequently the dc output of the filter will also be zero. On the other hand, when a frequency step is applied to the input, a phase error will be generated, resulting in a nonzero dc output as a function of the applied step as shown in Figure 6.27.

As an example, consider an input signal with initial frequency of 1 Hz. If a step of 0.2 is applied to the input, that is a frequency shift from 1 to 1.2 Hz, this will result in a phase shift of $\psi = 1.88$ rad $\equiv 108^o$ and the dc output is $\cos(1.88)/2 = -0.15$.

Another factor that affects the dc output is the amplitude of the input signal (denoted as A in (6.11)) which causes the detector dc to change. Therefore, the locking range of the EES-ATDTL is limited to a certain range of input amplitudes within which the FSM of the loop can operate properly as illustrated in Figure 6.27.

The proposed TDTL utilizes a variable gain block that is controlled by the FSM. Each value of the gain corresponds to a unique state of the of FSM, therefore

$$\phi(k+1) = \phi(k) - K_i^{'} h[\phi(k)] + \Lambda_o \tag{6.12}$$

where $K_i^{'} = \omega G_i$, G_i is a gain corresponds to a state i. If K_i is defined to be $\omega_o G_i$, then $K_i^{'} = K_i/W$, with $W = \omega_o/\omega$.

The operating conditions and simulation scenarios of the EES-ATDTL are similar to those of the SS-ATDTL. Therefore, the EES-TDTL in Figure 6.26 was tested by subjecting it to different frequency steps, which in the case of

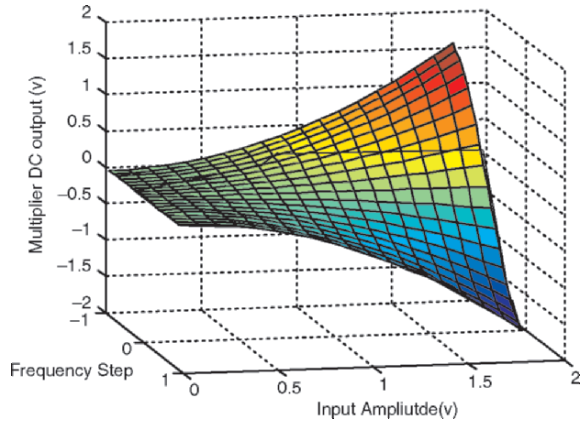
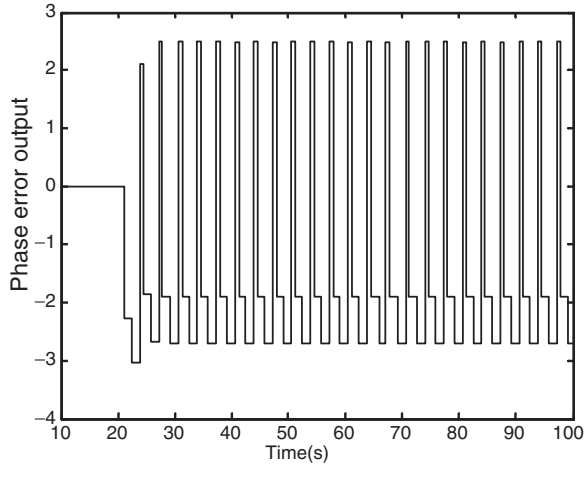


Figure 6.27: Characteristic function of the multiplier dc output. Delineated area shows the locking range of the loop in Figure 6.26.

the conventional TDTL can throw the system outside the locking range shown in Figure 6.22. The results of the simulation show that the loop responds and converges to a steady state phase error within few samples. These few samples correspond to the time taken by the newly introduced phase error detection circuit to respond. For example, a frequency step of -0.4 with $W = 1.6$, $K_1 = 1$ and $\psi_{o1} = \pi/2$ was applied to both the conventional and the new loop and their responses are shown in Figure 6.28. The locking performance of both loops is also demonstrated by the phase plane plots illustrated in Figure 6.29. The plots show that the conventional TDTL stays in the unlocked condition, whereas the new one converges into a steady state condition within an acceptable time.

6.4 Simulation Results of Second-Order TDTL

As was the case with the first-order TDTL, negative and positive frequency steps were applied to the second-order loop in order to observe its response. Figure 6.30 shows the response of the loop to a negative frequency step. The initial phase shift ψ_o is arranged as $\pi/2$ and K_1 is equal to unity. Referring to the second-order locking characteristics discussed earlier, it is obvious that the locking range is narrower and imposes restrictions on the choice of frequency ratios, making the second-order loop more susceptible to inputs causing instability.



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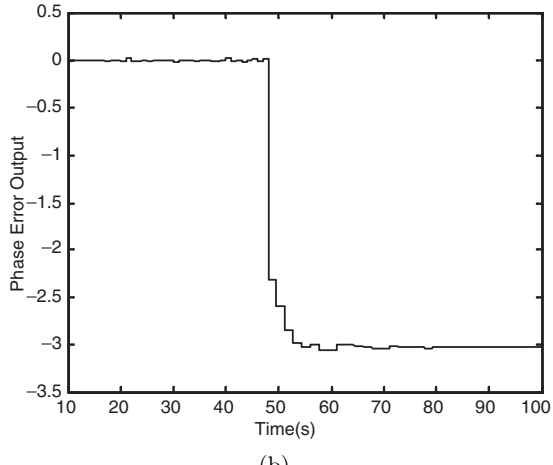
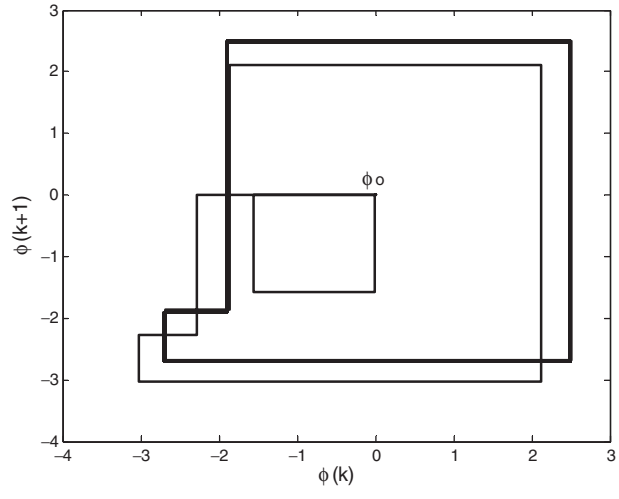
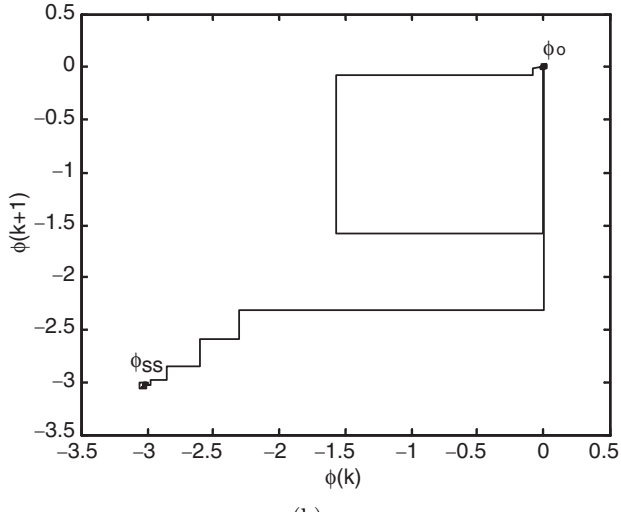


(b)

Figure 6.28: (a) The conventional TDTL response to a frequency step with $W = 1.6$ (b) The proposed TDTL response to the same frequency step.



(a)



(b)

Figure 6.29: (a) Phase plane of the conventional TDTL for a $W = 1.6$ (b) Phase plane of the proposed system for W=1.6.

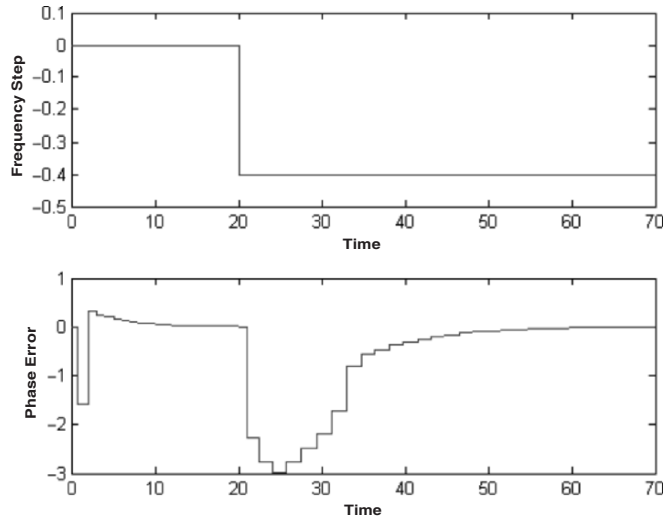


Figure 6.30: Tracking a negative frequency step with the second-order TDTL: (Top) input frequency step (Bottom) loop phase error.

The effect of applying an input signal with $W = 1.67$ to the loop, and the phase error response are shown in Figure 6.30. The most prevalent difference compared with the first-order loop is that the phase error converges to zero, i.e., the loop tracks both the frequency and the phase of the input signal. This fact is also confirmed in Figure 6.31, where it is clear the DCO samples are converging towards the positive going zero crossings of the input waveform.

The same behavior also applies for positive frequency steps as illustrated in Figure 6.32, in which a positive frequency step is applied to the second-order loop with the same set of parameters used in the negative step case. The phase error in this case converges to zero, causing the DCO to track the frequency and the phase of the input signal.

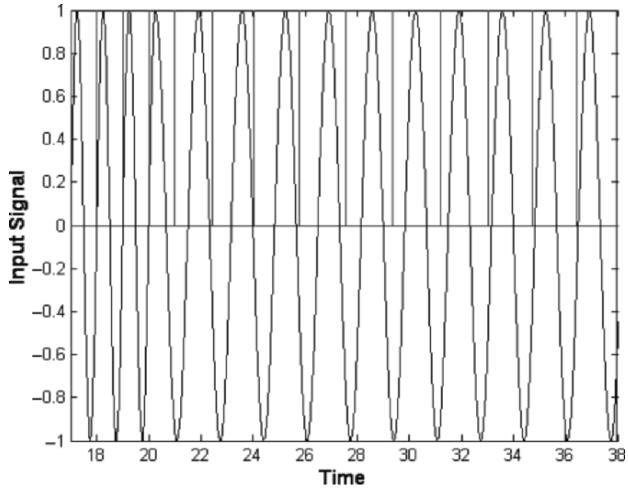


Figure 6.31: Sampling process of the second-order TDTL (negative step).

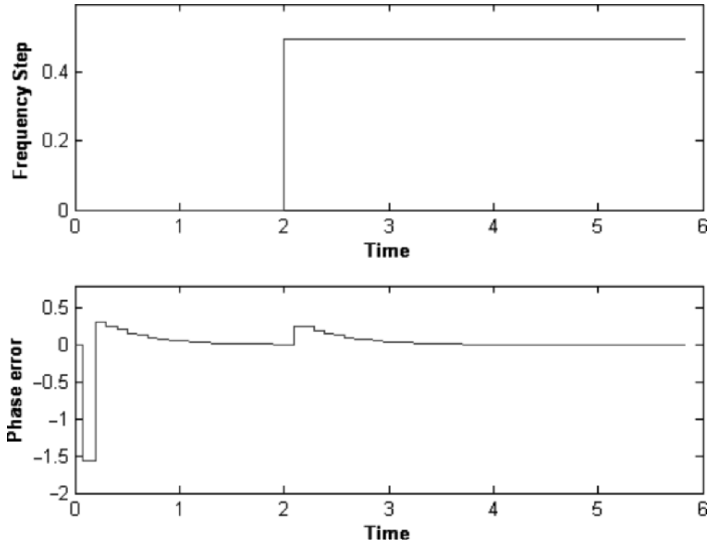


Figure 6.32: Tracking a positive frequency step with the second-order TDTL(Top) input frequency step (Bottom) loop phase error.

6.5 Improved Second-Order TDTL Architectures

This section discusses modified second-order TDTL architectures that improve the performance of the loop in terms of speed and locking range width. As in the case of the first-order, these modifications are based on the use of finite-state machines to control particular loop parameters and hence achieve the desired performance. The proposed architectures and their associated simulation results are described in the subsections below.

6.5.1 Adaptive Filter Coefficients Second-Order TDTL

In the fixed bandwidth TDTL, if the system is thrown out of lock due to a sudden change in the input frequency it will stay out of lock unless an external signal forces the digital controlled oscillator (DCO) back into the locking region. The TDTL can retain the lock state if it was always kept within the locking boundaries, and this can be achieved by adapting the coefficients of the filter in response to frequency steps, which will cause large errors.

The Adaptive Filter Coefficients Second-Order TDTL, shown in Figure 6.33, is created by utilizing digital filter with its coefficients controlled by an appropriate FSM. The FSM states are defined by the input phase error signal $e(k)$ and the output control signals $d(k)$ and $g(k)$. The phase error serves as an indicator of the operating point of the TDTL, therefore, the FSM can decide on the value of the filter coefficients G_1 and G_2 which will keep the loop inside its locking boundary. Since the system can acquire frequency steps such as point A in Figure 6.34, that is resulted from an input signal frequency with lower frequency than the DCO free running frequency ω_o, i.e., $W > 1$, the FSM keep the filter coefficients the same and does not alter them. When the system is subjected to a frequency step that causes the input signal frequency to go higher than ω_o, i.e., $W < 1$ such as point C in Figure 6.34, the FSM will update the control signals $d(k)$ and $g(k)$ in order to choose the appropriate values of G_1 and G_2 that ensure operating within the locking boundary of the loop.

The system in Figure 6.33 was tested by subjecting it to a step input change in frequency that pushes the loop to point C in Figure 6.34, where $W = 0.75$ and $K_1 = 1$, and comparing its behavior with that of the conventional second-order TDTL. The conventional loop goes into unlocked state and does not recover. However, the modified architecture in Figure 6.33 senses the error through its FSM and accordingly changes the digital filter coefficients so that the operating point is pushed to point I, which is within the locking boundary of the second order loop. The settling behaviors of the conventional loop as well as the adaptive filter coefficients second-order loop to the above step frequency input are illustrated by the transient responses in Figure 6.35 and the phase

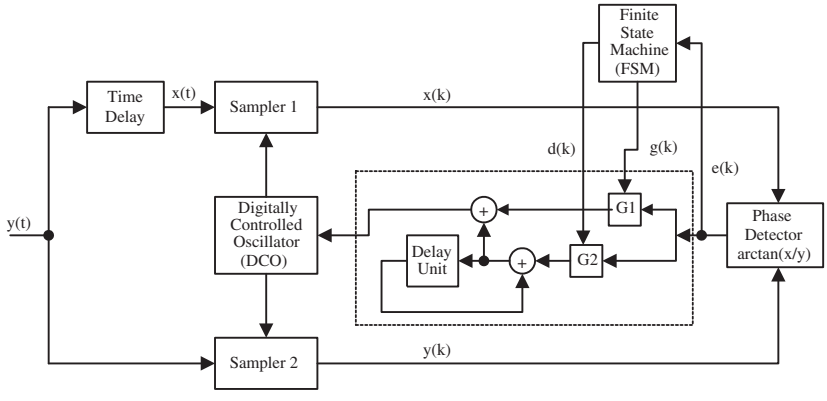


Figure 6.33: Adaptive filter coefficients second-order TDTL Architecture.

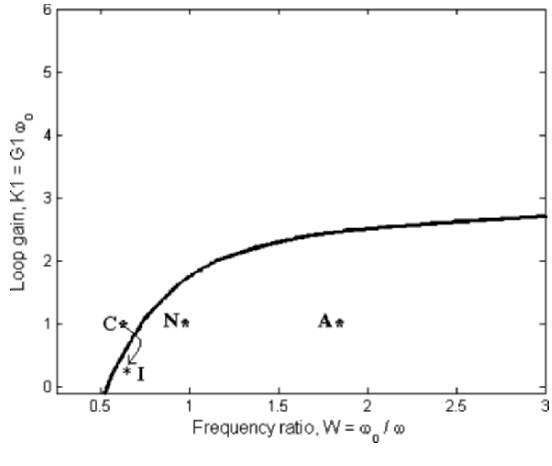


Figure 6.34: Locking range of adaptive gain second-order TDTL.

plane plots in Figure 6.36. Both figures show that when the loop is at point I, it converges into a steady state condition, whereas, when it is at point C, it stays in the unlock condition.

6.5.2 Adaptive Loop Gain Second-Order TDTL

The Adaptive Loop Gain Second-Order TDTL shown in Figure 6.37 offers wider locking range than the conventional second-order TDTL. The adaptive loop is designed to operate at the nominal point N, where $K_1 = 1$ and $W = 1$, shown in Figure 6.38 [107]. As the frequency changes around the carrier, i.e., $1 < W$ or $W > 1$, the loop is maintained in lock by the FSM block by changing the DCO frequency and the loop filter coefficients in order to keep $K_1 = 1$.

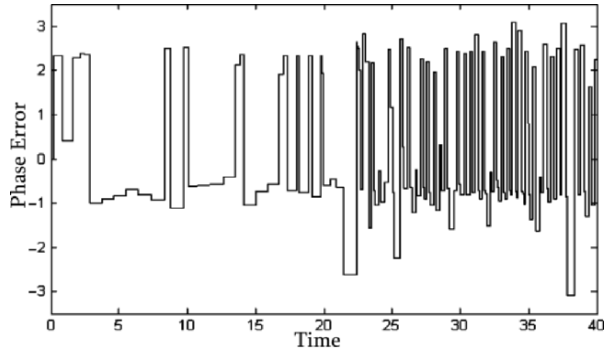
The FSM block has two inputs, $e(k)$ and $y(k)$. The criterion for state transitions is based on the magnitude of $e(k)$ and the sign of $y(k)$. The outputs of the FSM are the control signals $d(k)$ and $g(k)$, where $d(k)$ decides the operating frequency of the DCO and $g(k)$ decides the values of the filter coefficients that keeps the loop gain $K_1 = 1$.

The Adaptive Loop Gain Second-Order TDTL was evaluated by subjecting it to different frequency steps. The extensive results produced indicate that the adaptive TDTL has an improved locking performance when compared to the conventional TDTL. This can be illustrated by applying a frequency step that takes the loop to a point B of Figure 6.38, where $W = 0.58$ and $K_1 = 1$. This frequency step will drove the conventional Second Order TDTL out of lock as shown by the transient response and the phase plane Figure 6.39.

The locking performance of the adaptive loop gain system for the same frequency step is shown in the phase plane plot shown in Figure 6.40. It can be seen that, while the system in Figure 6.37 manages to settle through its adaptation mechanism within acceptable time when applying the same frequency step to it, the conventional second order TDTL failed to do so because of its limited locking range.

6.6 A Variable Order TDTL Architecture

The Variable Order TDTL, shown in Figure 6.41, enhances the performance of the original loop by utilizing the wide bandwidth of the first order loop and the high signal to noise ratio with zero steady state phase error of the second order loop. This is achieved by varying the order of the digital filter block within the TDTL and hence changing the overall order of the loop in order to maintain acquisition status.



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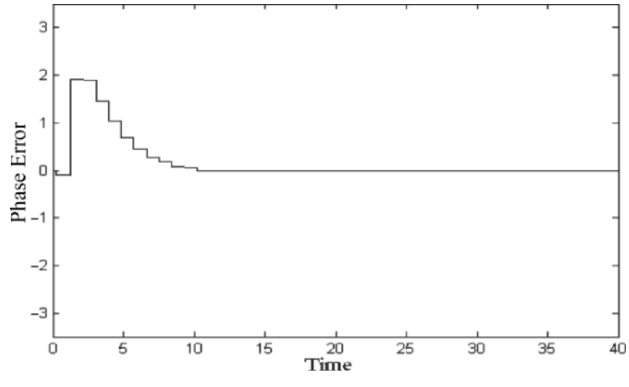
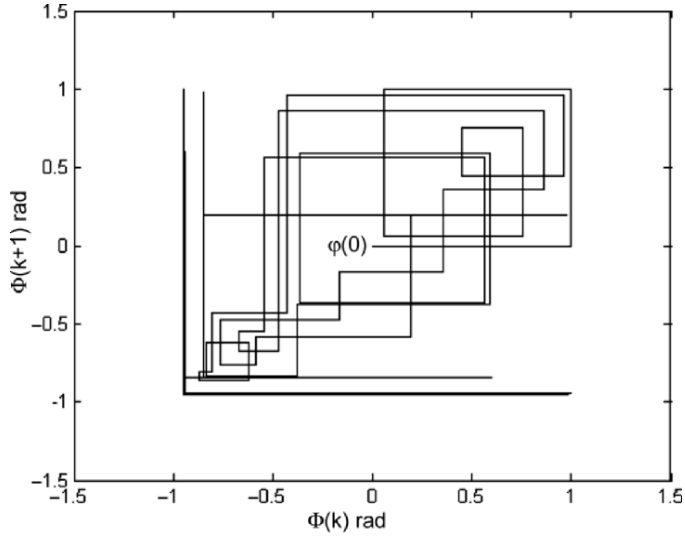
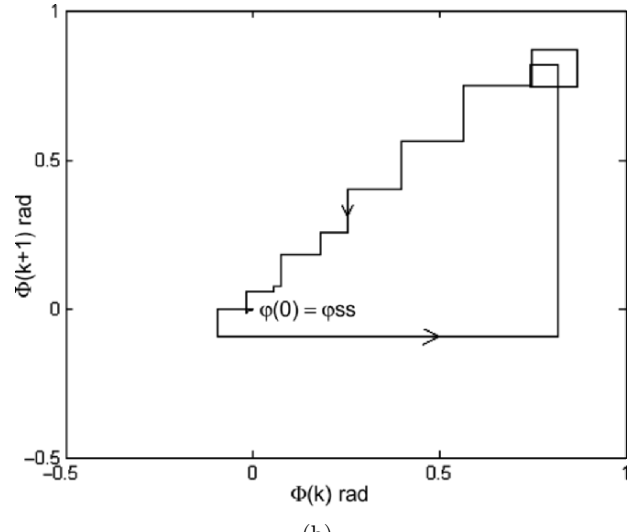


(b)

Figure 6.35: Transient response of (a) Conventional second-order TDTL (b) Adaptive filter coefficients second-order TDTL.



(a)



(b)

Figure 6.36: Phase plane plots of (a) Conventional second-order TDTL (b) Adaptive filter coefficients second-order TDTL.

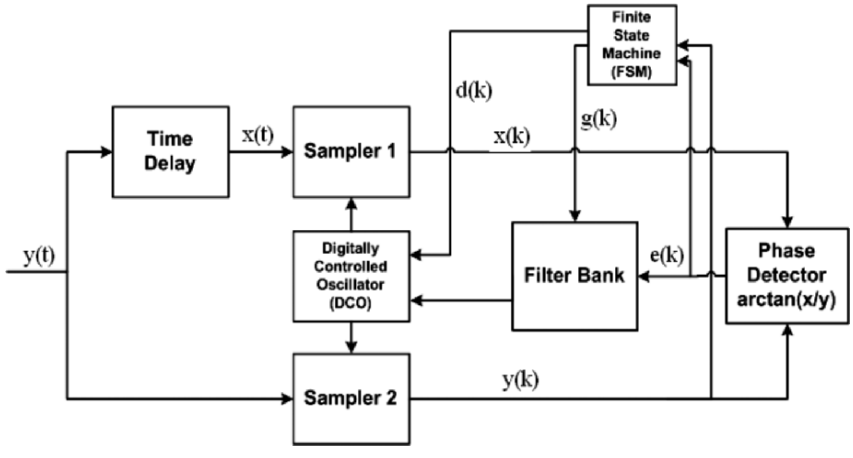


Figure 6.37: Adaptive loop gain second-order TDTL architecture.

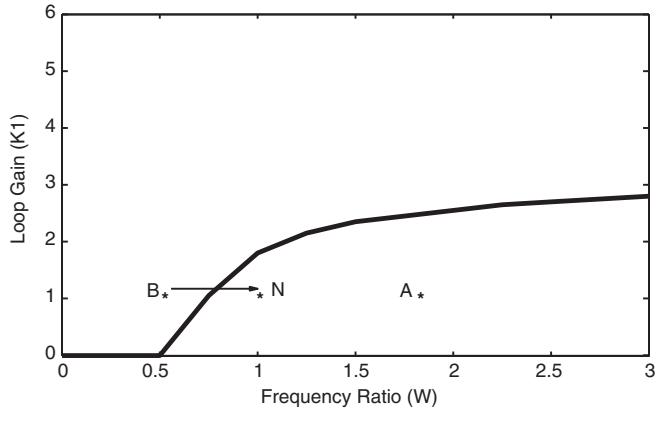
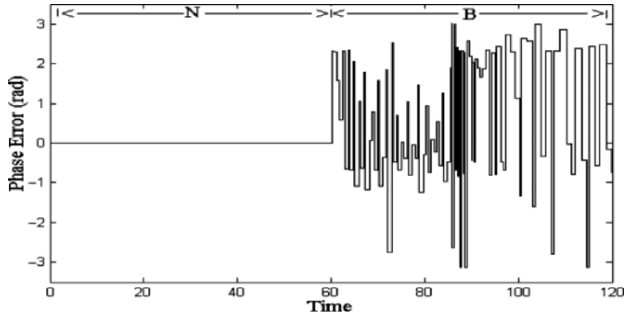
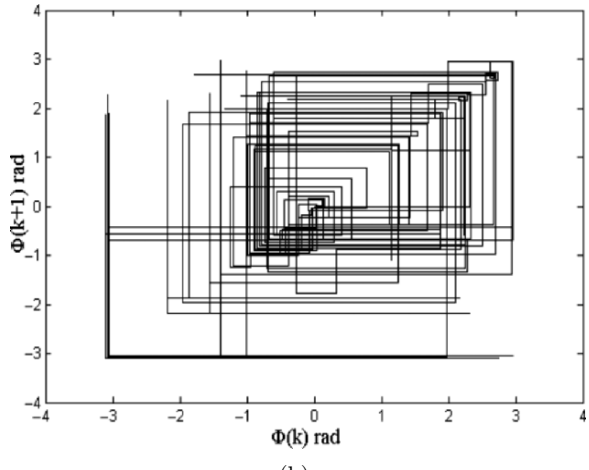


Figure 6.38: Locking range of adaptive second-order TDTL.



(a)



(b)

Figure 6.39: (a) Conventional second-order TDTL (a) Transient response (b) Phase plane.

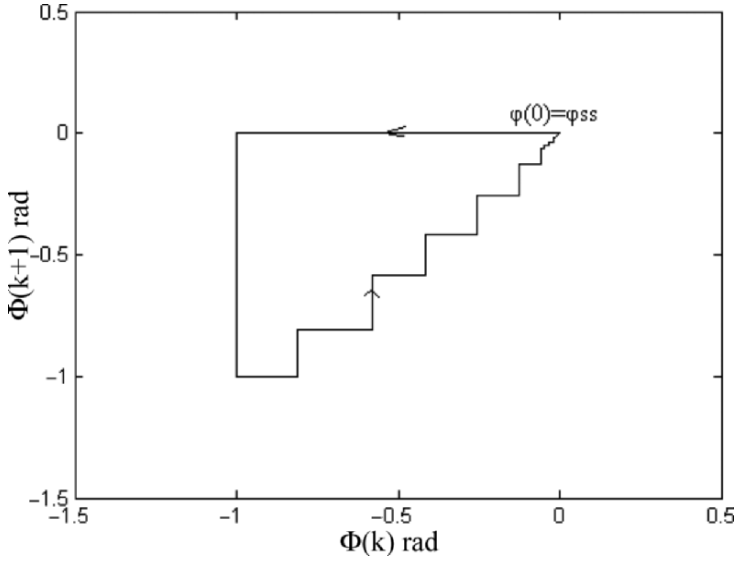


Figure 6.40: Phase plane of the adaptive loop gain second-order TDTL.

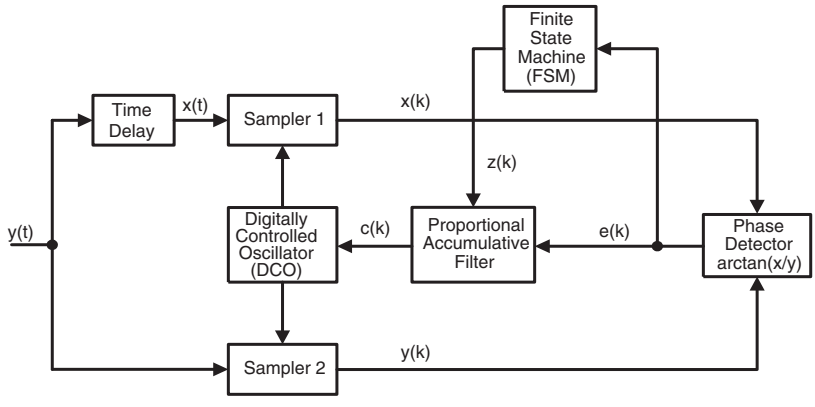


Figure 6.41: Variable order TDTL structure.

The loop in Figure 6.41 is similar to the conventional TDTL structure except for the filter bank and the use of the FSM block. The FSM decides on the filter order that is to be used in order to provide the best achievable locking on the input signal according to the introduced frequency disturbances. The system is designed to operate at point N of Figure 6.42, where $K_1 = 1$ and $W = 1$, with the second-order loop as a default order due to its zero steady state phase error and high SNR.

Due to its narrow bandwidth, the second order TDTL is more susceptible to inputs with higher frequency than the DCO free running frequency, which will cause more instability than the first order loop. The loop architecture in Figure 6.41 combines both the first-order and second-order loops to get a more reliable system with zero steady state error and high SNR when the frequency step is within the locking range of the second order TDTL and a stable system with a small steady state error when it is outside the locking range of the second order loop.

The FSM in Figure 6.41 senses the phase error signal and switches from second order to first order TDTL whenever the frequency step exceeds a predefined positive threshold that is on the boundaries of the locking range of the second order loop. The FSM also switches the loop back to the second order TDTL mode when the effect of the frequency step is either omitted or reduced to within the locking range boundaries of the second order loop. This loop mode control mechanism of the Variable Order TDTL results in an improved locking range compared with single mode loop as shown in Figure 6.42.

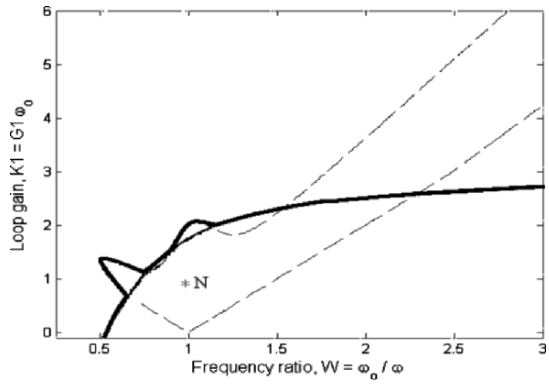


Figure 6.42: Variable order TDTL locking range with $\psi_{o1} = \pi/2$.

As mentioned in the previous chapter, VO-TDTL combines first- and second-order TDTLs in order to enhance the locking performance of the loop and improves its noise immunity to frequency disturbances. The first-order TDTL provides fast acquisition and hence improved locking range, and the second-order loop offers high signal to noise ratio and zero steady-state error, which makes the DCO follow the input signal frequency very closely.

We will take $K_1 = 1$ and assume two points, A at $W > 1.5$ and B at $W < 0.75$. The settling behavior of the first order TDTL at those points is shown in Figure 6.43. Point A is selected to be outside the locking range of the first-order TDTL, therefore, the loop stays in the unlock condition. The phase plane plot of Figure 6.44 demonstrates this. The phase plane plot of Figure 6.45 shows the loop locking performance at point B. It shows that when the disturbance is within the locking boundaries of the loop, it converges to a steady state condition within acceptable time.

Testing the second-order TDTL response at the same set of points with the same K_1 and referring to the loop locking characteristics resulted in the settling behavior an shown in Figure 6.46. The phase plane plot of Figure 6.47 shows the loop locking performance at point A. It can be seen that the phase started at zero and after few samples it reached to the steady state phase error value, where it converged to zero. Since point B is outside the second order loop locking range which resulted in the unlock condition shown in the phase plane plot of Figure 6.48.

Due to the previously mentioned desirable features of the second order TDTL for many communication applications, the proposed system works as a second order TDTL until the loop is subjected to a large positive frequency step causing the second order TDTL to go outside the locking range such as point B with $W < 0.75$. The system senses this error through its FSM and switches to

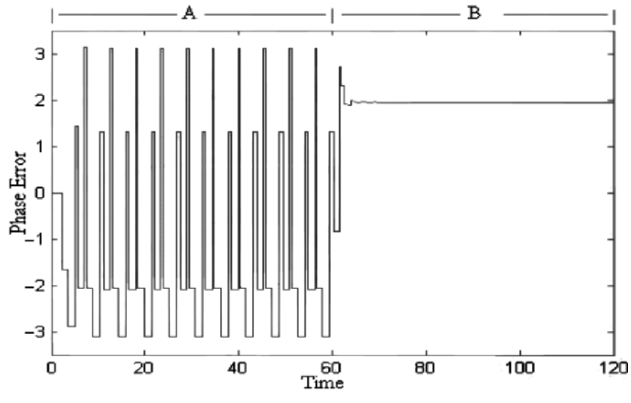


Figure 6.43: Transient response of the first-order TDTL at points A and B.

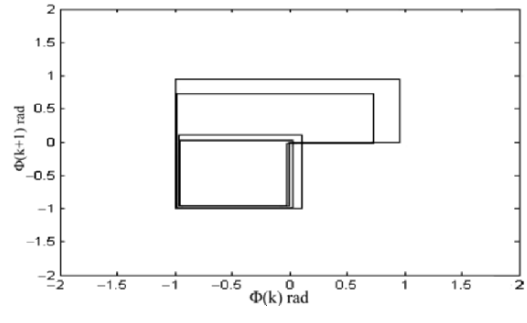


Figure 6.44: Phase plane at point A.

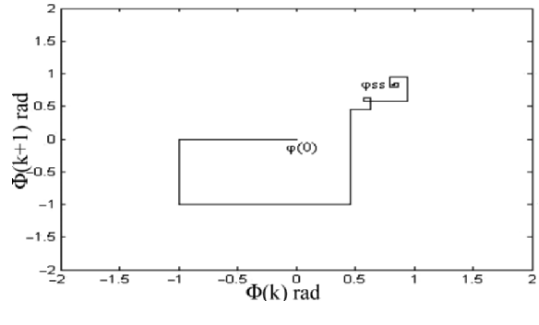


Figure 6.45: Phase plane at point B.

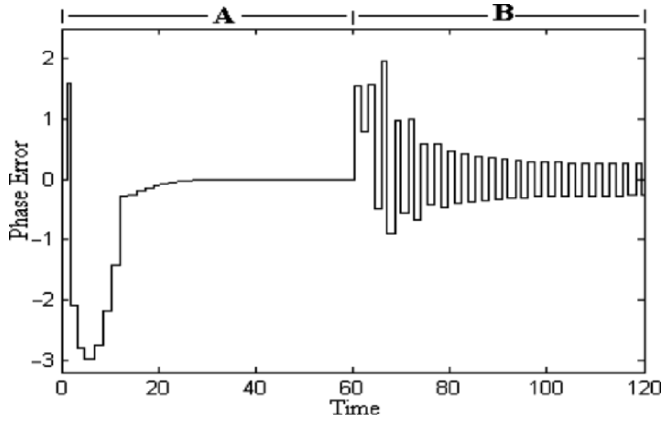


Figure 6.46: Transient response of the second-order TDTL at points A and B.

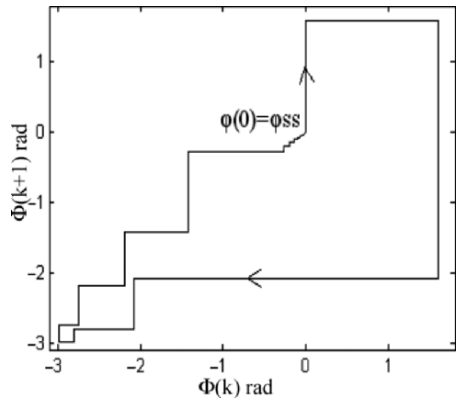


Figure 6.47: Phase plane at point A.

the first order loop, which brings the loop to the locking state. The system also monitors the frequency disturbances until it is reduced to an amount that can be handled by the second order TDTL, where the FSM switches the loop back to second order. With reference to Figure 6.42, the transient response of the Variable Order TDTL for a sequence of frequency steps that take the operating point of the loop to points A and B respectively is shown in Figure 6.49. The variable order TDTL improves the performance of the loop and provides a wide symmetrical locking range for acquiring both positive and negative frequency steps.

In addition to the TDTL architectures discussed in this book, a technique that widens the locking range for both first and second order TDTLs was reported in [112]. It achieves this through modification of the free running sampling rate and the digital filter output.

6.7 Conclusions

In this chapter we presented the simulation results of the original TDTL and compared them with those obtained from the improved TDTL architectures. The objectives of the improved architectures were to enhance the overall performance of both the first-order and second-order TDTL systems. The results illustrated that the new architectures achieved the desired objectives with varied degrees of success.

For the first-order TDTL the following improved architectures were presented: delay switching, adaptive gain, combined delay switching and adaptive

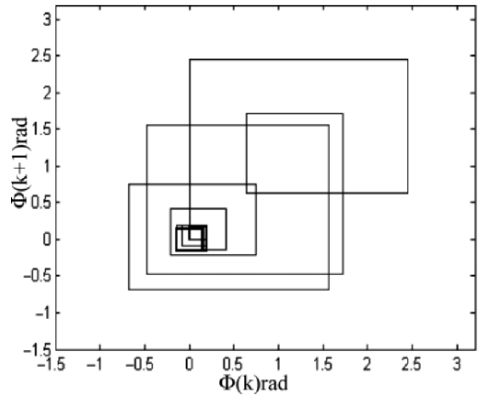


Figure 6.48: Phase plane at point B.

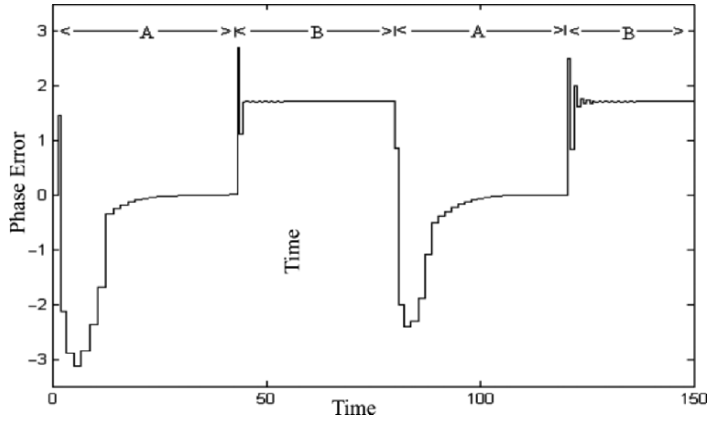


Figure 6.49: Transient response of the variable order TDTL at points A and B.

gain, sample sensing and early error sensing. The combined delay switching and adaptive gain architecture results in the best improvement in the TDTL locking range, while the early error sensing architecture enhances the acquisition time of the loop.

In the case of the second-order TDTL, the adaptive filter coefficients and the adaptive loop gain architectures were shown to improve the system performance. The results indicate that the two architectures have comparable performance, with the adaptive loop gain having marginally faster acquisition capabilities.

We finally presented the variable order architecture that harnessed the desirable characteristics of the first-order and second-order TDTLs. The variable order architecture achieved a wide locking ranged compared with the fixed order loop. However, under fast switching conditions the loop performance tends to get degraded.

Chapter 7

FPGA Reconfigurable TDTL

Some of the TDTL architectures that were presented earlier were implemented on a reconfigurable field-programmable gate array (FPGA) based system. The synthesis and subsequent implementation process required the conversion of the loop blocks to hardware realizable circuitry. This chapter gives an overview of reconfigurable computing systems and then presents a brief introduction to FPGA technology, which is the main driver of reconfigurable systems. This is followed with a detailed discussion of the process of converting the TDTL Matlab/Simulink models to FPGA implementation and the real-time results that were obtained.

7.1 Overview of Reconfigurable Systems

In traditional computing systems, the execution of algorithms is carried out by two dominant methods. The first is to perform the operation in hardware via the use of an Application Specific Integrated Circuit (ASIC). As these ASICs are designed and well optimized to specifically perform a given computation, they are very fast and efficient when executing the exact computation for which they were designed. However, once fabricated these circuits cannot be altered because they are hard-wired.

On the other hand, microprocessor based systems execute algorithms with a high degree of flexibility. In this method, the processor performs the required computations by executing a set of instructions. The functionality of processor-based systems can be easily changed by simply changing the software instructions or program without making any form of alteration to the hardware. However, the performance of microprocessor-based system is far below that of an ASIC. The reason being that the processor performs computation by completing a fetch-decode-execute cycle for each instruction; which involves

reading an instruction from memory, interpreting it and then executing it. The net result is a high execution overhead for each individual operation.

Reconfigurable computing is a paradigm for system design that is intended to fill the gap between the hardware and software computing systems discussed above. Its primary aim is to achieve higher performance than software, while maintaining a higher level of flexibility than hardware. Reconfigurable computing utilizes hardware modules that can be adapted at run-time to facilitate greater flexibility without compromising performance. Reconfigurable architectures can exploit fine-grain and coarse-grain parallelism available in the application due to their adaptability. Exploiting this parallelism provides significant performance advantages compared with conventional microprocessors. The reconfigurability of the hardware permits adaptation of the hardware for specific computations in each application to achieve higher performance compared to software [86, 88].

Complex functions can be mapped onto the architecture achieving higher silicon utilization and reducing the instruction fetch and execute bottleneck. Due to their inherent parallelism and reconfigurability, FPGAs are currently the main building blocks of reconfigurable computing systems for a wide range of applications [91]. The application areas of FPGA-based reconfigurable systems include digital communications, digital signal processing, communication security, high performance computing and many others. The next section presents an overview of FPGA architectures.

7.2 FPGA Structure and Operation

FPGAs are general-purpose digital integrated circuits that consist of programmable or configurable logic blocks along with configurable interconnects between these blocks. Depending on the implementation technology used, some FPGAs may be programmed a single time, while others may be reprogrammed as many times as needed. In all cases, FPGA programming is done by the user hence the "field programmable" part of the FPGA's name. The configurable aspect of FPGAs is one of the main factors that differentiate them from ASICs.

The general structure of an FPGA is shown in Figure 7.1. It contains three major types of resources: logic blocks, input/output (I/O) blocks to connect to the chip pins, and interconnection wires and switches. The logic blocks, which may include dedicated look-up tables (LUTs), registers, multipliers, dual port memories, tri-state buffers, multiplexers, digital clock managers and others, are arranged in a two-dimensional array that can be configured to implement a wide range of arithmetic and logic functions. The interconnect wires are organized in dedicated horizontal and vertical routing channels between rows and columns

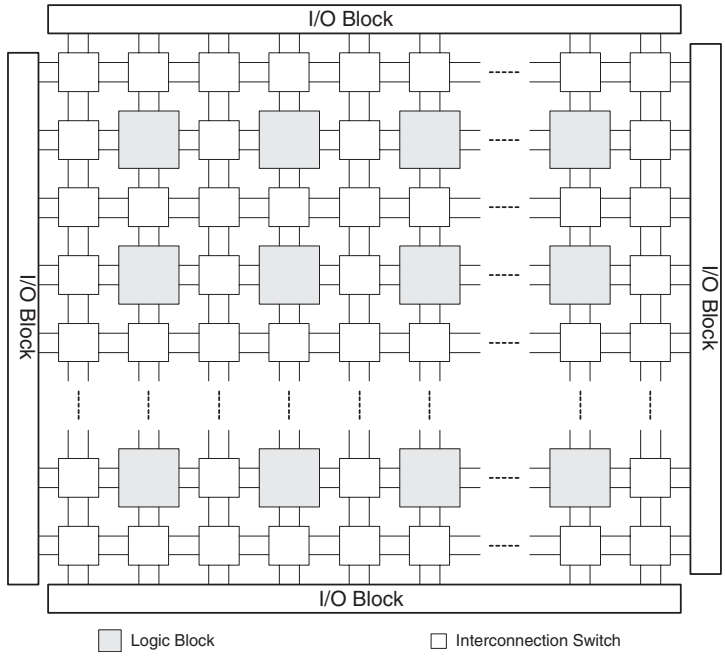


Figure 7.1: General structure of an FPGA.

of logic blocks. The routing channels contain wires and programmable switches that allow the computing logic blocks and I/O resources to be linked in various ways to form systems under the control of the device configuration bitstream. [92, 93, 94].

FPGA performance is derived from the ability they provide to construct highly parallel architectures for processing data. In contrast with a microprocessor or DSP processor, where performance is tied to the clock rate at which the processor can run, FPGA performance is tied to the amount of parallelism that can be brought to bear in the application algorithms. A combination of increasingly high system clock rates and highly distributed memory architectures give the system designer an ability to exploit parallelism in processing of data streams.

All FPGAs need to be configured or programmed in order to synthesize the required digital system. There are three major circuit technologies for configuring an FPGA: SRAM, antifuse, and flash. These technologies are discussed briefly below.

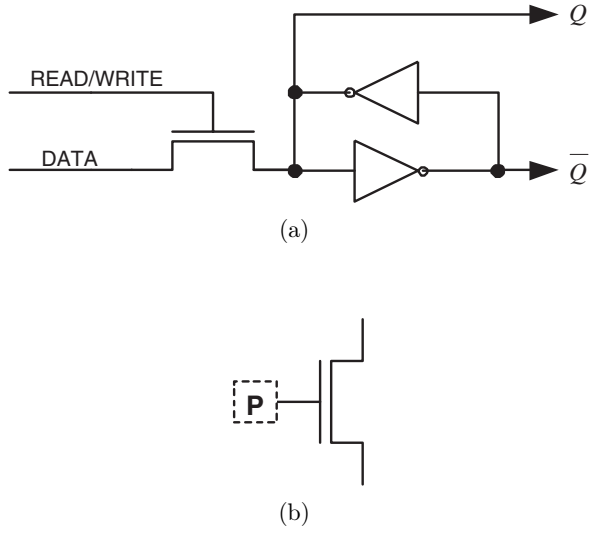


Figure 7.2: (a) Programming SRAM Cell. (b) Programmable routing connection.

Static RAM (SRAM): In SRAM-based FPGAs programmable connections are made using transmission gates, or multiplexers that are controlled by SRAM cells. Figure 7.2 depicts an SRAM-based programmable cell [96]. The output (Q) in Figure 7.2-a drives the input (P) of the programmable routing connection in Figure 7.2-b. In SRAM technology devices can be configured dynamically over and over again. This distinct property results in many advantages that include: new ideas can be quickly implemented and tested, it allows fast in-circuit reconfiguration, and an FPGA can be programmed to perform self-test or system test as well as its main task. Furthermore, SRAM-based FPGA are at the forefront of technology and that enables them to benefit from the technological developments in standard SRAM manufacturing. The major disadvantage of SRAM-based FPGAs is that they have to be reconfigured every time the system is powered up. This requires the use of a special external memory device, which adds to the cost and size of the overall system. Another disadvantage is that SRAM cells are larger than antifuses and flash cells.

Antifuse: An anti-fuse resides in a high-impedance state, and can be programmed into low impedance or "fused" state. Figure 7.3 shows an antifuse device before and after programming [94]. Antifuses are one-time programmable devices, which when "blown" create a via-connection, while when "unblown" act

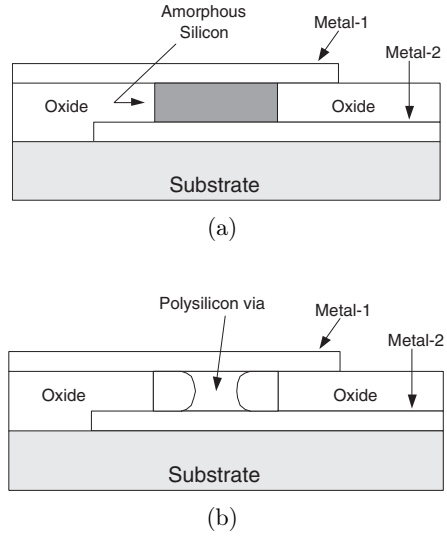


Figure 7.3: Antifuse Device (a) Before Programming (b) After Programming.

as an open circuit with very high resistance. The disadvantage of this technology is that it is one time programmable and offers less design flexibility compared with SRAM technology. The main advantage of antifuse-based FPGAs is that their configuration information is non-volatile, which means they do not need to be reconfigured on power up.

Flash: Flash memory is a form of EEPROM (electrically erasable programmable ROM) that can be rapidly erased. Flash uses a floating-point gate structure in which a low-leakage capacitor holds voltage that controls a transistor gate. Components based on flash have a variety of architectures. Figure 7.4 shows a possible flash programmed cell [95, 108]. The main advantage of flash-based FPGAs is that they can be reprogrammed without external storage for reconfiguration. However, flash devices require five additional processing steps more than SRAMs and they tend to have high static power dissipation.

The vast majority of FPGAs are based on SRAM technology due to their flexibility and ease of reconfigurability as outlined above. The remainder of this chapter will use SRAM-based FPGAs.

Figure 7.1 showed an abstract top-view of an FPGA. Each logic block in Figure 7.1 has a small number of inputs and one output. In most FPGAs the logic block is a look-up table (LUT), which contains SRAM cells and multiplexers. An n-input LUT can implement any possible n-input combinational logic function. Figure 7.5 illustrates a three-input LUT. It has eight SRAM cells because

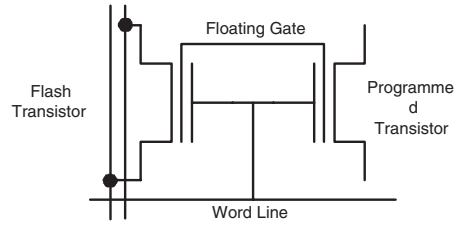


Figure 7.4: Flash Based FPGA Switch.

the truth table of a three-variable function has eight rows. Adding more inputs allows an LUT to represent more complex functions. Most current FPGAs tend to use 4-input LUTs as they offer an optimal balance of device utilization and performance. The multiplexers in an LUT are normally implemented in the form of transmission gates.

The LUT is combined with other components to form the core building block of an FPGA. In the case of Xilinx FPGAs this is called a logic cell (LC). As shown in Figure 7.6, an LC consists of a 4-input LUT, which can also act as 16x1 RAM or a 16-bit shift register, a multiplexer and a register. The register can be configured to act as a flip-flop or a latch.

In the case of Xilinx FPGAs, joining two LCs results in what is called a slice as illustrated in Figure 7.7. The LUT, multiplexer and register in each LC have their own data inputs and outputs. However, the slice has one set of clock, clock enable and set/reset signals that are common to both LCs.

The highest level of the hierarchy in Xilinx FPGAs is called a configurable logic block (CLB) [96, 97]. Depending on the particular FPGA device, a CLB consists of either two or four slices. Figure 7.8 shows a 4-slice CLB. A complete CLB represents a single logic block of those shown in Figure 7.1. The CLB schematic of an actual Xilinx 4000 FPGA series is shown in Figure 7.9 [96].

7.3 Xtreme DSP Development System

The Xtreme DSP Development Kit-II was the implementation platform of the reconfigurable TDTL in this work. The development board, shown in Figure 7.10, is powered by a Virtex-II FPGA chip from Xilinx. In addition to that, it provides dual channel high performance analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), enabling the development of

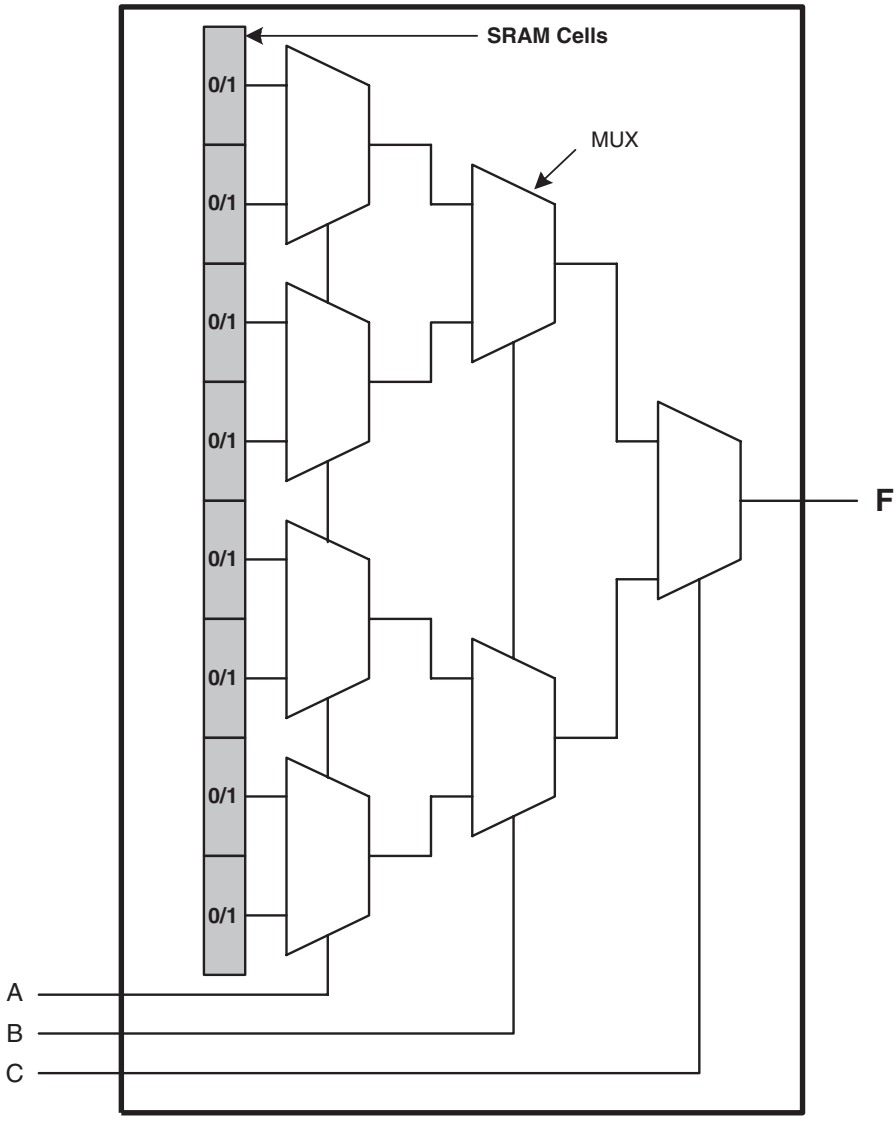


Figure 7.5: Three-Input LUT.

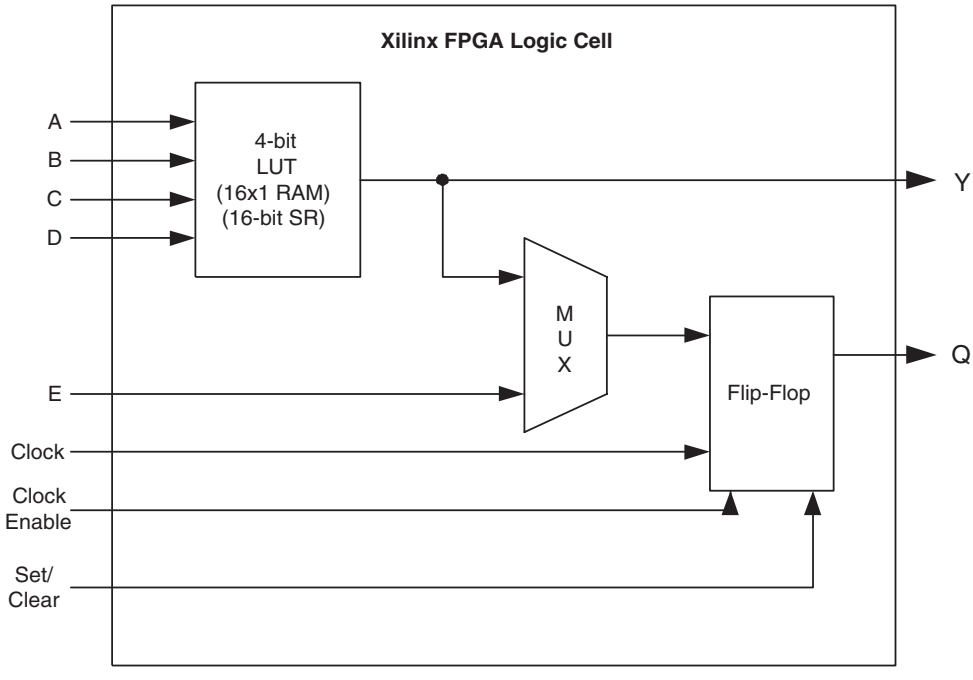


Figure 7.6: A simplified Xilinx FPGA logic cell.

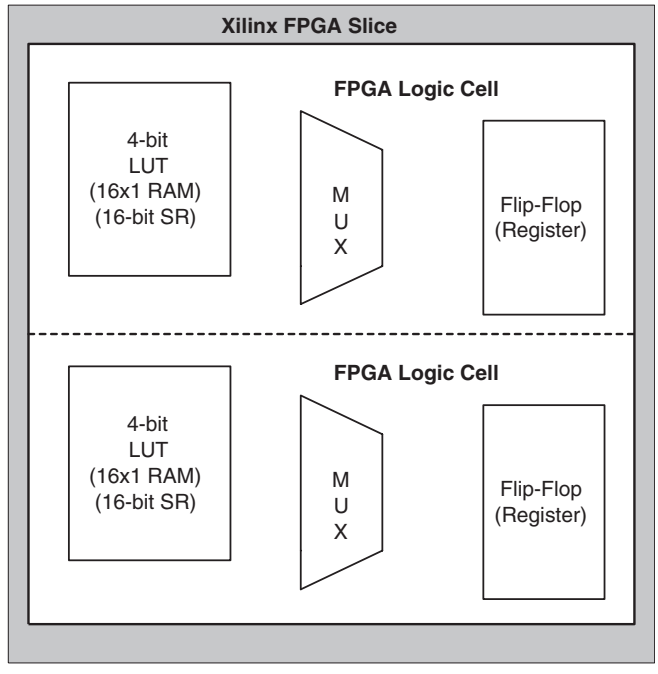


Figure 7.7: Xilinx FPGA slice.

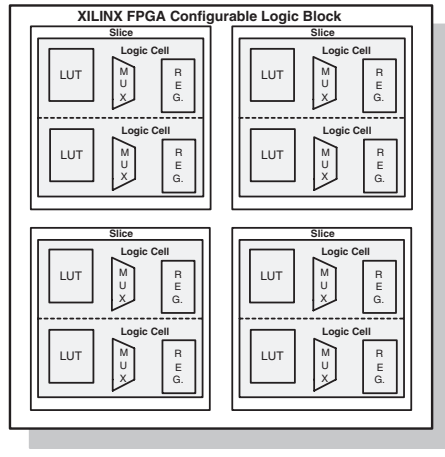


Figure 7.8: Configurable logic block.

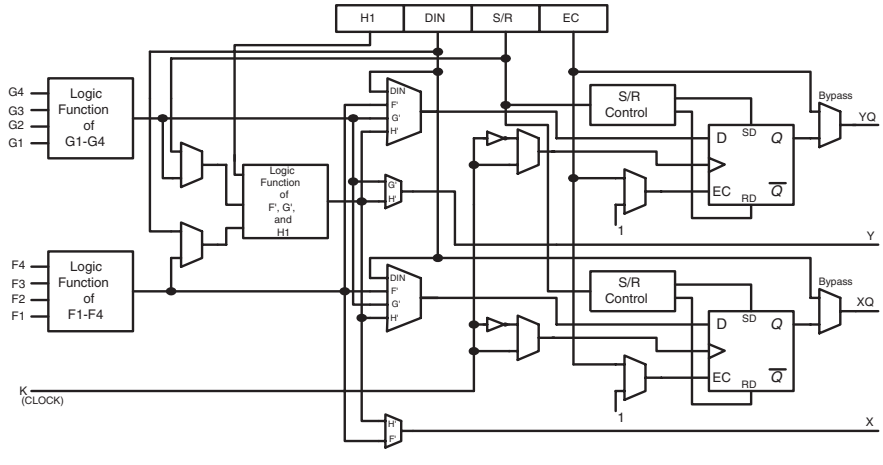


Figure 7.9: Configurable logic block of Xilinx 4000 Series FPGA.

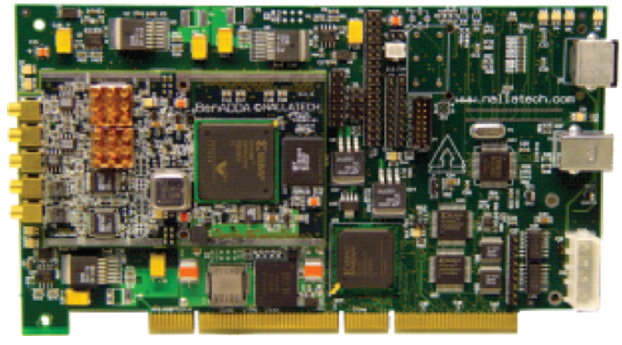


Figure 7.10: Xtreme DSP development board.

such applications as software defined radio, wireless networking, HDTV, video imaging and many others [98].

The block diagram of the Xtreme DSP development board is shown in Figure 7.11, where it is clearly seen that the board is composed from three Xilinx FPGA chips. The first is the Virtex-II XC2V3000, which has a capacity of three million gates. This chip is called the *Main User* FPGA, since it is used to implement the bitstreams developed by the user. The second FPGA chips is the Virtex-II XC2V80, which is configured by the user for the purposes of clocking and I/O management. The third FPGA is the Spartan-II interface FPGA, which is preconfigured for the purpose of communication with the PC using the PCI bus or the USB [98].

The Xilinx System Generator serves as the software development platform of the reconfigurable TDTL system. It consists of a MATLAB/ Simulink library called the Xilinx Blockset, and software to translate a Simulink model into a hardware realization of the model.

The System Generator maps system parameters defined in Simulink (e.g., as mask variables in Xilinx Blockset blocks), into entities and architectures, ports, signals, and attributes in a hardware realization. In addition to that, System Generator automatically produces command files for FPGA synthesis, hardware description language (HDL) simulation, and implementation tools, so that the user can work entirely in graphical environments in going from system specification to hardware realization [99].

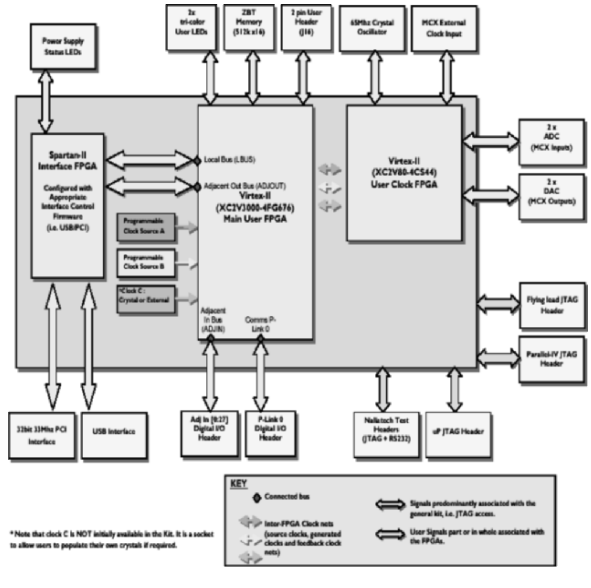


Figure 7.11: Xtreme DSP block diagram.

The Xilinx Blockset is accessible in the Simulink library browser, and elements can be freely combined with other Simulink elements. Only those subsystems denoted as Xilinx black boxes, and blocks and subsystems consisting of blocks from the Xilinx Blockset are translated by System Generator into a hardware realization.

The generation process is controlled from the System Generator block found in the Xilinx Blockset Basic Elements library. The System Generator parameterization graphical user interface (GUI) allows the user to choose the target FPGA device, target system clock period, and other implementation options. The System Generator translates the Simulink model into a hardware realization by mapping Xilinx Blockset elements into Intellectual Property (IP) library modules, inferring control signals and circuitry from system parameters (e.g., sample periods), and converting the Simulink hierarchy into a hierarchical VHDL netlist [98, 99].

Furthermore, the System Generator creates the necessary command files to create the IP block netlists using CORE Generator, invokes CORE Generator, and creates project and script files for HDL simulation, synthesis, technology mapping, placement, routing, and bit stream generation. To ensure efficient compilation of multi-rate systems, the System Generator creates constraint files for the physical implementation tools. The System Generator also creates an HDL test bench for the generated realization, including test vectors computed during Simulink simulation. A graphical representation of the design flow using the Xilinx System Generator is shown in Figure 7.12 [99].

7.4 TDTL FPGA Implementation

The implementation of the TDTL discussed in Section 3.2 into an FPGA requires the translation of the major components of the loop, which were previously modelled using MATLAB/Simulink blocks, into hardware-mappable blocks. After that, these blocks can be simulated on a bit and cycle true basis and then complied into a HDL script. Xilinx System Generator includes plenty of these blocks, and these were used to modify the architecture of the TDTL into the reconfigurable model shown in Figure 7.13.

The reconfigurable TDTL, shown in Figure 7.13, has undergone some modification in order to optimize the utilisation of resources. While the TDTL shown in Figure 3.1 suggests using two sample and hold (S/H) or ADC circuits, this implementation is expensive in terms of size, cost and power consumption. Thus, the TDTL was modified to include a single ADC sampled at the system clock rate, which is much higher than the free running frequency of the loop. The ADC digitizes the continuous-time input signal so that further processing, including the delay operation, can be carried out digitally. In addition to

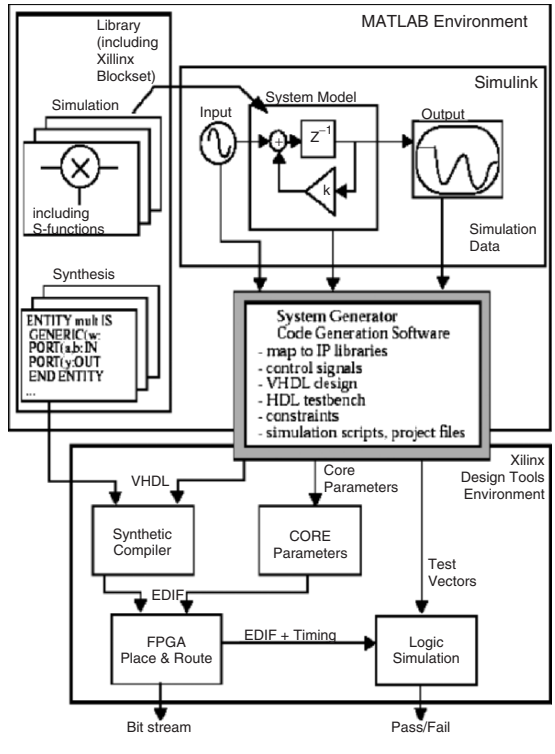


Figure 7.12: Design flow using Xilinx System Generator.

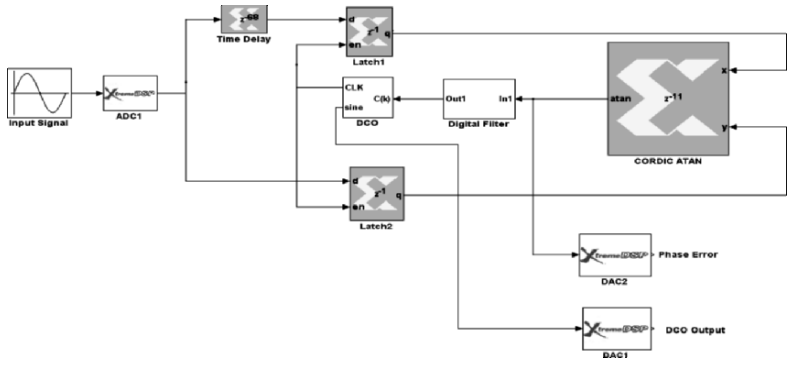


Figure 7.13: Reconfigurable FPGA-based TDTL implementation.

that, each S/H block can be replaced by a latch, as shown in Figure 7.13. The latches perform the same conceptual function as that of S/H blocks in Figure 3.1; however, they are operating fully in the digital domain.

The DAC blocks are used to propagate the phase error and the output of the DCO to the outside world, in order to observe the performance of the loop and perform data acquisition and logging. The following subsections will explain the major components of the reconfigurable TDTL.

7.4.1 The CORDIC Arctangent Block

The COordinate Rotational DIgital Computer (CORDIC) algorithm is an iterative method of calculating trigonometric and hyperbolic functions using mainly shift and add operations. This feature made the algorithm an attractive option for hardware implementation. Specifically, it lends itself for the architecture of FPGAs in applications such as digital signal processing, digital control, filtering and matrix algebra [100].

The CORDIC algorithm is used to implement the 4-quad $\text{Tan}^{-1}(x/y)$ function of the phase detector, converging to angles between $\pm\pi$ within eleven system clock cycles. The architecture of the CORDIC arctangent block is shown in Figure 7.14.

The CORDIC $\text{Tan}^{-1}(x/y)$ algorithm is implemented in 3 steps:

Step 1: Coarse Angle Rotation. At this stage, the algorithm converges only for

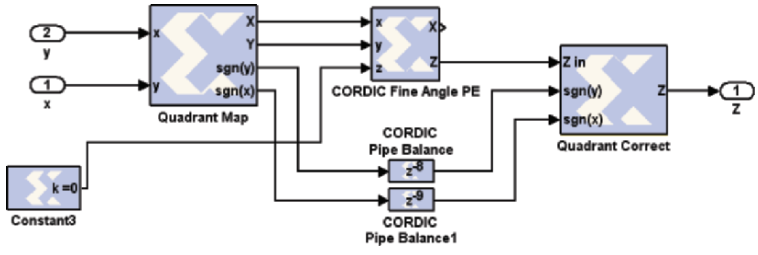


Figure 7.14: CORDIC implementation of $\text{Tan}^{-1}(x/y)$ function.

angles between $-\pi/2$ and $\pi/2$, so that if $x < 0$, the input vector is reflected to the 1st or 3rd quadrant by making the x-coordinate non-negative.

Step 2: Fine Angle Rotation. For rectangular-to-polar conversion, the resulting vector is rotated through progressively smaller angles, such that y goes to zero. In the i^{th} stage, the angular rotation is by either $\pm\arctan(1/2^i)$, depending on whether or not its input y is less than or greater than zero.

Step 3: Angle Correction. If there was a reflection applied in Step 1, this step applies the appropriate angle correction by subtracting it from $\pm\pi$ [101, 102].

7.4.2 The Digital Controlled Oscillator

The architecture of the DCO is of great influence on the performance of the loop. Usually, DCOs are implemented by using modulo-m or divide-by-m counters. These counter circuits are clocked by a high frequency source, and the output frequency of the counter source frequency divided by the control word m. The disadvantage of using such counter is the poor frequency resolution. Therefore, it was not preferred as a choice of DCO implementation.

The DCO was implemented using a Direct Digital Synthesis (DDS) block, which can be described as a frequency-controlled synthesizer of sinusoidal waveforms. The DDS block diagram is shown in Figure 7.15 [103]. The idea of direct digital synthesis revolves around storing the values of a sinusoidal waveform

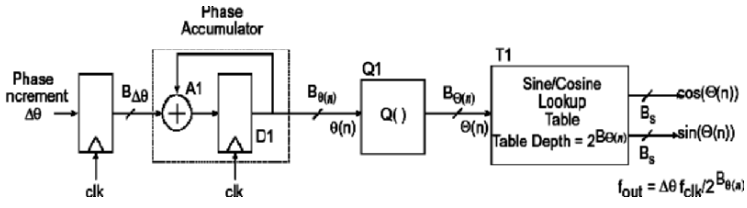


Figure 7.15: Block Diagram of the DDS Block.

over a quarter of a cycle in a look-up table (LUT), which maps a certain phase argument to produce the output waveform.

As shown in Figure 7.15, the phase increment, which can be thought of as the digital word determining the output frequency, is received and then applied to a phase accumulator consisting of adder A1 and register D1. The slope of the phase accumulator is then mapped to a sinusoid by the look-up table T1. However, the high precision output of the phase accumulator is reduced to a low precision one which matches the input width of the look-up table. This is performed using the quantizer Q1 and presents the slope to the address port of a look-up table that performs the mapping from phase-space to time. The quality of a signal formed by recalling samples of a sinusoid from a look-up table is affected by both the phase and amplitude quantization of the process. The length and width of the look-up table affect the signal's phase angle resolution and the signal's amplitude resolution respectively [103].

The output frequency of the DDS is a function of the system clock frequency f_{clk}, the number of bits $B_{\theta(n)}$ in the phase accumulator and the phase increment value $\Delta\theta$. The output frequency f_{out} can be calculated in Hertz as follows

$$f_{\text{out}} = \frac{f_{\text{clk}}\Delta\theta}{2^{B_{\theta(n)}}} \tag{7.1}$$

The DDS block is capable of providing fine frequency resolutions reaching up to 0.02 Hz at $f_{\text{clk}} = 100$ MHz. Another advantage of using the aforementioned block is the regeneration of the sinusoidal input to the TDTL directly and without the need for extra processing blocks, which is not possible with other architectures. The DCO pulses, which trigger the latches, can be created by squaring up the output of the DDS block. In addition to that, extra logic gates are required to form an edge detection circuit as shown in Figure 7.16, and this is due to the fact that the latch blocks provided by Xilinx Blockset are level

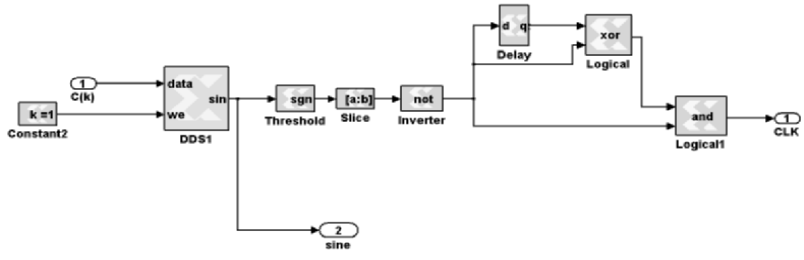


Figure 7.16: Implementation of the DCO.

triggered. Hence, they will stay active during the high state of the DCO pulses, unless the formers become high only during transitions.

The free running frequency of the loop f_o has been set to 250 KHz, and this requires a phase increment $\Delta\theta_o$ of 2^{12} , for a system clock of 65 MHz. The input phase increment is the result of adding $\Delta\theta_o$ with the modified output of the digital filter $c(k)$, therefore the output frequency of the DCO can be defined as

$$f_{\text{out}} = \frac{f_{\text{clk}}[\Delta\theta + c(k)]}{2^{B_{\theta(n)}}} \tag{7.2}$$

7.4.3 The CORDIC Divider

As mentioned above, the output frequency of the DCO will be updated according to (7.2). However, this violates the condition stated in Section 3.2, which states that the period of the DCO is to be updated at each sampling instant according to (3.5), which is given again below

$$T(k) = T_o - c(k-1).$$

Therefore, in order for the DCO to function properly, the output of the digital filter, which will be denoted as $c^{\Lambda}(k)$ must be mapped through the following function in order to obtain the required output $c(k)$

$$c(k) = -\Delta\theta_o \left(1 + \frac{1}{c^{\Lambda}(k) f_o - 1}\right) \tag{7.3}$$

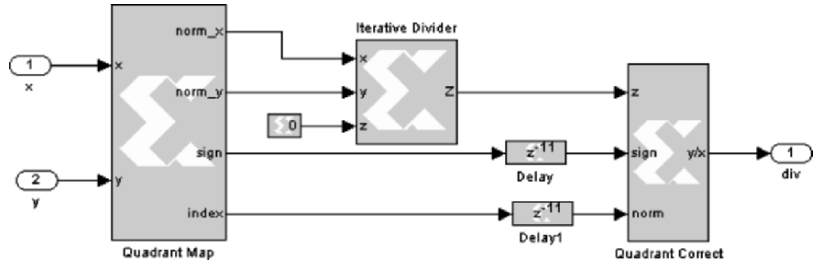


Figure 7.17: CORDIC divider implementation.

Equation (7.3) above must be implemented in hardware in order to bridge the output of the digital filter with the input of the DCO. The equation requires addition, multiplication and division operations. While the first two can be easily implemented using fixed-point hardware, the third one is the most complex and demanding in terms of hardware implementation. Several algorithms can be used to perform non-power-of-two division, and the one used in the synthesized system is the CORDIC divider shown in Figure 7.17.

The steps involved in the implementation of the CORDIC divider algorithm are as follows:

Step 1: Co-ordinate Rotation. The CORDIC algorithm converges only for positive values of x, so if $x <$ zero, the input vector is reflected to the 1^{st} or 3^{rd} quadrant by making the x-coordinate non-negative. For normalizing x and y, y is always mapped to a non-negative value. The Divider circuit has been designed to converge for all values of x and y, except for the most negative value.

Step 2: Normalization. The CORDIC algorithm converges only for y greater than or equal to *2x*. For x greater than y, both the inputs x and y are shifted to the left till they have a 1 in the most significant bit (MSB). The relative shift of y over x is recorded and passed on to the Quadrant Correct Stage.

Step 3: Linear Rotations. For ratio calculation, the resulting vector is rotated through progressively smaller angles, such that y goes to zero. In the i-th

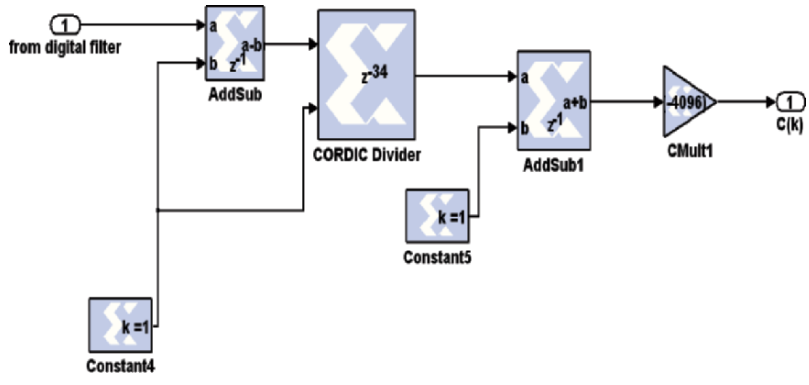


Figure 7.18: Hardware Implementation of Equation (7.3).

stage, the rotation yields $\pm\ y/x$, depending on whether the input y is less than or greater than zero.

Step 4: Co-ordinate Correction. If the axis was rotated Step 1 and a relative shift was applied to y over x, this step assigns the appropriate sign to the resulting ratio and multiplies it with $2^{(\text{relative shift of y/x})}$ [101, 102]. This operation is expensive in terms of complexity and time, since it consumes 34 system clocks, and therefore it imposes restrictions on the free running frequency of the TDTL. The hardware realization of (7.3) is shown in Figure 7.18.

7.5 Real-Time TDTL Results

The following sub-sections present some of the real-time results that were achieved following the FPGA conversion and subsequent implementation of some of the TDTL architectures that were discussed in Chapter 7. The results include those of the first-order TDTL, second-order TDTL and the sample-sensing adaptive TDTL. The performance of the reconfigurable TDTL implemented in this section are compared with those obtained through simulations earlier in order to ascertain that the overall functionality of the synthesized systems is acceptable. Complete verification of embedded phase lock loops requires the application of more tests as discussed in [109].

7.5.1 First-Order TDTL

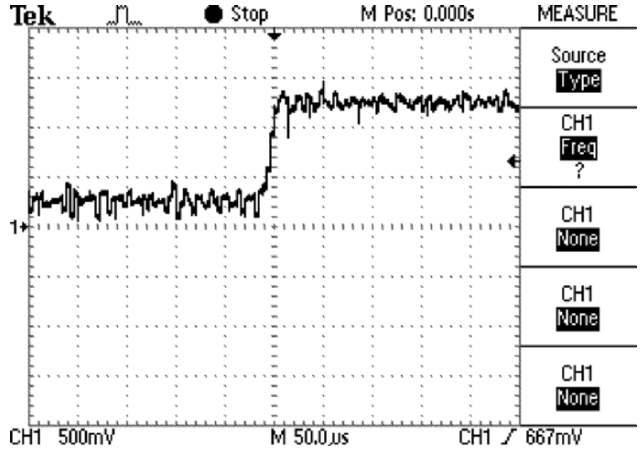
The first-order loop is designed by multiplying the output of the phase detector with G_1. The loop gain K_1 has been selected as unity, therefore, G_1 will be equal to $1/2\pi = 0.1592$. In order to induce a nominal phase shift of $\pi/2$ to the input signal, the time-delay unit should be equal to quarter the period of f_o, namely 1 microsecond. Since the smallest delay possible is equal to the period of the system clock (1/65 MHz), the number of delay stages required is the ratio between the time delay and the system period, which is approximately equal to 68 in this case. The implementation of the TDTL has consumed a total of 54,751 gates out of the total capacity of the Virtex-II, which is around 3 million system gates.

Figure 7.19-a shows the behaviour of the phase error when the first-order reconfigurable TDTL is subjected to a positive frequency step. In this case, the initial input frequency was 260 KHz, and a sudden increase caused the input frequency to rise to 280 KHz. As the figure shows, the TDTL follows the change in frequency and settles rapidly. An interesting observation in the captured phase error is the existence of noise-like ripples, which contradict with the theoretical simulations shown in Figure 7.19-b, in which the phase error is smooth in its steady state condition.

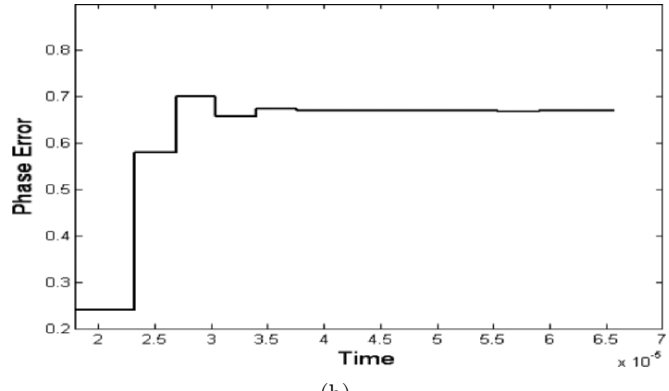
The ripples in the real-time response of Figure 7.19-a do not indicate that the loop is out of lock. In fact they are the result of various practical factors not taken into consideration in the simulation. These are mainly caused by quantization noise, which is related to the resolution of the ADC, the truncation and calculation errors, since the loop is performing critical calculations in hardware using a limited number of bits. The limited frequency resolution of the DCO also introduces errors in calculations, and it can be stated that a ripple free output requires a synthesiser with a frequency resolution that approaches minus infinity [110].

7.5.2 Second-Order TDTL

The second-order TDTL shares the same implementation issues with the first order loop except for the digital filter, which is implemented as a proportional accumulative (PA) filter with the transfer function described in section 3.3.2. The loop gain has been chosen as 1.5 with a nominal phase shift of $\pi/2$. The hardware implementation of the PA filter is shown in Figure 7.20, and the total gate count of the implemented second order loop was equal to 55940 gates. Due to the existence of an accumulator in the digital filter, it is expected that the truncation and calculation errors are also going to accumulate at each clock cycle, causing the performance to be very sensitive to frequency changes, and in most cases oscillatory.



(a)



(b)

Figure 7.19: Transient response of the first-order TDTL for a frequency step from 260 KHz to 280 KHz. (a) Actual real-time response. (b) Simulated response.

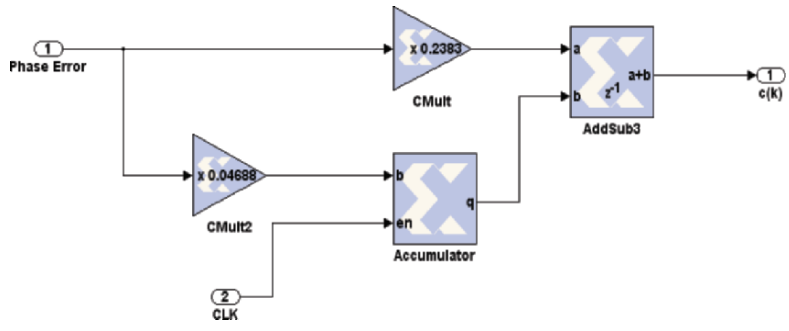
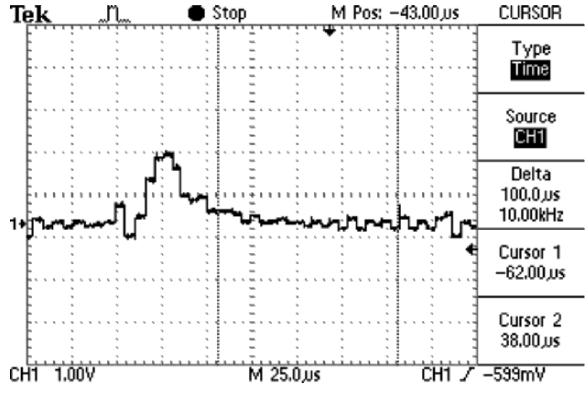


Figure 7.20: Realization of the PA loop filter.

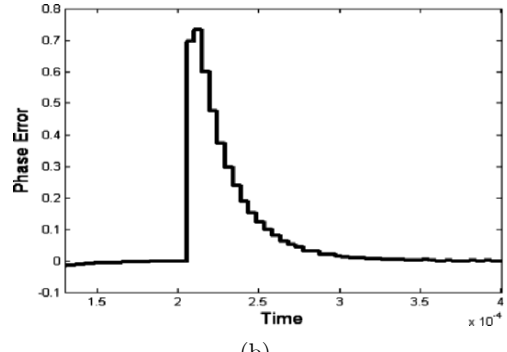
Since the phase error of the second-order loop is always converging to zero for inputs within its lock range, the existence of a frequency step can be read from the phase error output by observing the existence of sudden impulses that will slowly decay to a steady state level. This is demonstrated by the real-time response in Figure 7.21-a, where the input frequency of the implemented TDTL was suddenly increased from 175KHz to 205KHz. The decaying positive impulse is obvious, so is the effect of error accumulation, where it is clear that the oscillations are growing with time after the step was subjected to the loop. Figure 7.21-b depicts the theoretical response of the second-order TDTL to the same frequency step. The error accumulation is negligible in the theoretical response since all calculations are done using double precision arithmetic operations.

7.5.3 Sample Sensing Adaptive TDTL

The sample sensing adaptive first-order TDTL (SS-ATDTL) discussed in Chapter 6 was converted for FPGA implementation as shown in Figure 7.22. The architecture in Figure 7.22 includes a finite state machine (FSM) block. In this work, the FSM was designed using Moore state machine approach, which consists of mainly the next state logic, state register and output logic. The System Generator provides different methods for implementing Moore FSM, such as using block and distributed memory, using Black box block with VHDL instructions or using MCode block to implement the transition function, and



(a)



(b)

Figure 7.21: Transient response of the second-order loop for a frequency step from 175 KHz to 205 KHz. (a) Actual real-time response. (b) Simulated response.

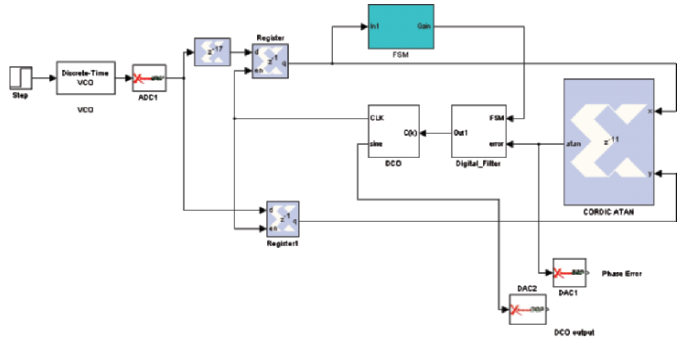


Figure 7.22: FPGA Implementation of sample sensing adaptive first-order TDTL.

registers to implement state variables. The last method was used to implement the FSM as it gives more flexibility and support using Matlab instructions in the design of the logic. Figure 7.18 shows the hardware implementation of the FSM.

The behaviour of the SS-ATDTL shown in Figure 7.22 was studied by subjecting it to various frequency steps and comparing it with that of the TDTL in Figure 7.23. The real-time results of the FPGA-based systems to a positive frequency step that changed from 140KHz to 156KHz are illustrated in Figure 7.24. From the figure, it can be clearly seen that SS-ATDTL settles rapidly while the TDTL gets out of lock. This confirms the simulation results discussed in Chapter 6.

7.6 Conclusions

This chapter presented an overview of the field of reconfigurable computing and the FPGA technology that is used to implement such systems. It then detailed the design flow of the Xtreme DSP system that was used to implement reconfigurable TDTLs.

The process of implementing the TDTL on an FPGA required the transformation of the MATLAB/ Simulink model to one that is FPGA synthesizable. Following the transformation process the first-order, second-order as well as some of the improved architectures of each type were downloaded to the FPGA based Xtreme DSP system and real-time results were illustrated. Comparison of the real-time results with those obtained from MATLAB/ Simulink simulations

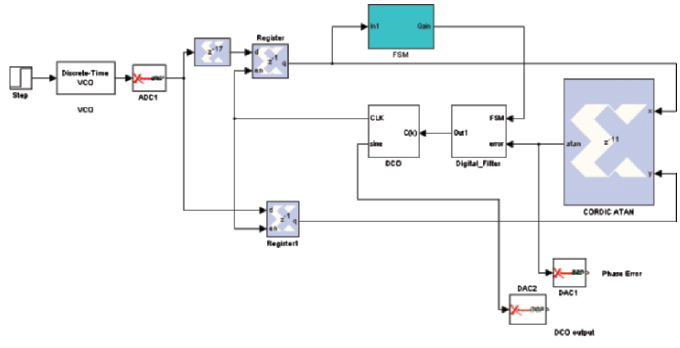
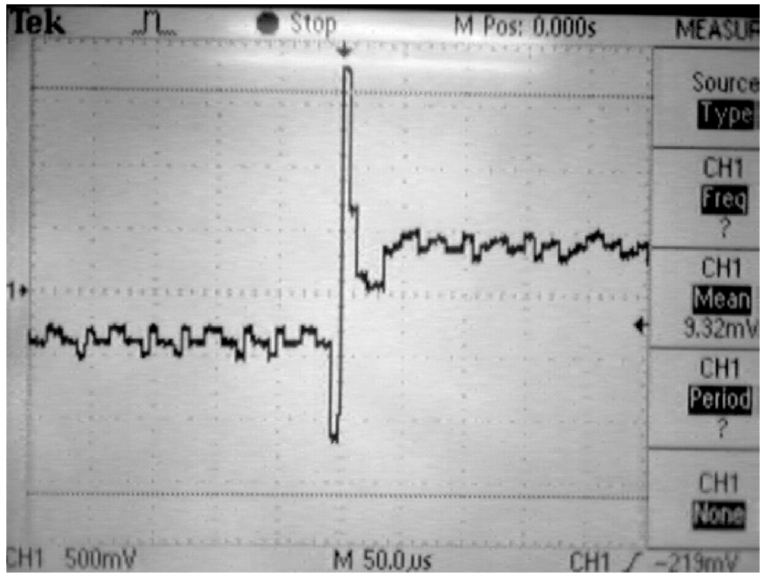
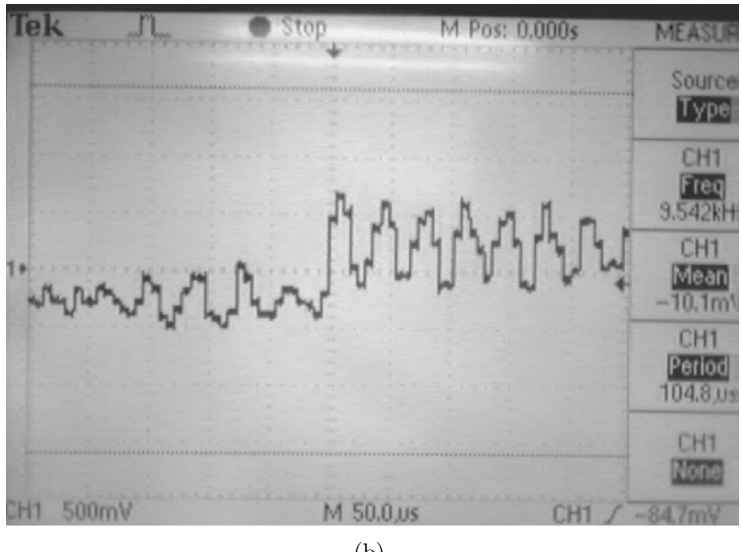


Figure 7.23: FSM hardware implementation.

indicates that they are broadly in agreement. In addition to illustrating the feasibility of implementing the TDTL on an FPGA, the above results show the flexibility of reconfigurable systems and advantages they offer in applications such as software defined radio.



(a)



(b)

Figure 7.24: Positive frequency step transient response of the (a) SS-ATDTL and (b) TDTL.

Chapter 8

Selected Applications

The previous chapters discussed in detail the structure, mathematical model and behaviour of the TDTL. We also presented a number of architectures that enhanced the performance of the loop and showed the process of implementing the TDTL on an FPGA based reconfigurable system. Synchronization and frequency tracking remain as the main applications of any DPLL in communications or signal processing. In addition, we further investigate in this chapter the capability of the TDTL in demodulating angle-modulated signals in the presence of additive Gaussian noise. Significant improvement over analog techniques of nearly 20 dB is obtained [104]. This is mainly due to the to its fast locking performance and its less sensitivity to amplitude variation. The TDTL was also tested for real time demodulation of FSK as well as wide band FM as will be shown in the following sections.

8.1 PM Demodulation Using TDTL

PM signals convey the information message $m(t)$ in the phase of a sinusoidal carrier with center frequency $\omega_o = 2\pi f_o$ such that the phase is linearly proportional to the message as follows

$$x(t) = A_o \sin[\omega_o t + \Delta_p m(t) + \gamma_o] \tag{8.1}$$

where Δ_p is a constant called the phase sensitivity and γ_o is the initial phase. For testing purposes we will consider the message to be a single-tone signal $m(t) = A_m \sin(\omega_m t)$ such that the PM signal will be

$$x(t) = A_o \sin[\omega_o t + \beta \sin(\omega_m t) + \gamma_o] \tag{8.2}$$

where $\beta = A_m \Delta_p$ is the modulation index and γ_o is a constant.

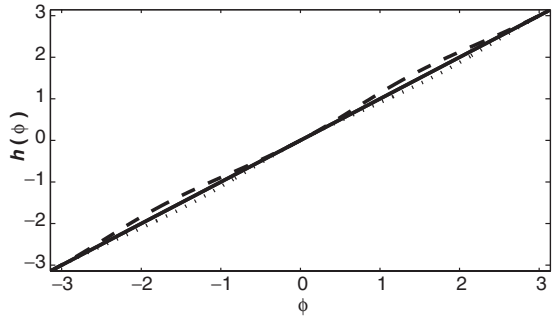


Figure 8.1: Characteristic function of the time-delay digital tanlock loop (TDTL) when $\psi_o = \pi/2$. Solid line is for the frequency ratio $W = \omega_o/\omega = 1$, dashed line for $W = 1.1$, and dotted line for $W = 0.9$.

Now we consider the characteristic function of the TDTL $h(\phi)$, which is a non-linear function as shown in (3.15) except in the case when $\psi_o = \pi/2$ and $W = \omega_o/\omega = 1$, which gives $h_\psi(\phi) = \phi$. If we arrange $\psi_o = \pi/2$, then for small values of the phase error $\phi(k)$ (which can be ensured in case the frequency ratio $W = \omega_o/\omega$ is inside the lock range), the TDTL characteristic function can still be approximated by (8.3) and as shown in Figure 8.1

$$h_\psi(\phi) \approx \phi \ \text{ for small } \phi. \tag{8.3}$$

Now if we arrange the parameter K_1 in (3.16) of the first-order TDTL to be 1 and the carrier frequency to be the loop center frequency ω_o, then by using equations (3.9), (3.13), (3.16), (8.1), and (8.3) it can be shown that

$$m(k) \approx \frac{1}{\Delta_p} \sum_{i=0}^{k} e(k) + \gamma_o. \tag{8.4}$$

Hence, a PM signal can be demodulated by adding up the PED output samples then using a low-pass analog filter for reconstruction as shown in Figure 8.2. However, this is true only if the incoming frequency range is inside the locking range. In Chapter 3, the locking conditions of the first-order TDTL were given by:

$$2|1 - W| \ < \ K_1 \ < 2W \, \frac{\sin^2(\alpha) + \sin^2(\alpha + \psi_o/W)}{\sin(\psi_o/W)}$$

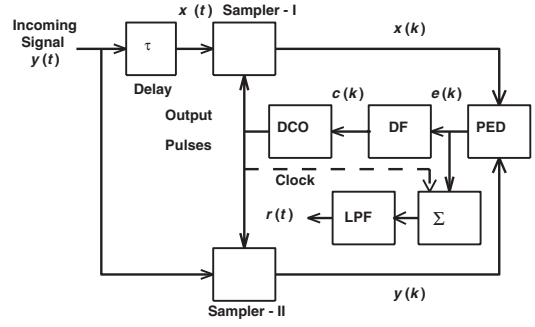


Figure 8.2: Block diagram of the TDTL PM-demodulator. Bold lines represent multi-bit connections.

where

$$\begin{aligned} \alpha &= \tan^{-1}(\rho) \\ \rho &= \frac{\sin(\psi)\tan(\zeta)}{1-\cos(\psi)\tan(\zeta)} = \frac{\sin(\psi)}{\cot(\zeta)-\cos(\psi)} \\ \zeta &= e_{ss} = f[\mathrm{Tan}^{-1}(\frac{\sin(\phi_{ss})}{\sin(\phi_{ss}+\psi)})] = \frac{\Lambda_o}{K_1'} \end{aligned}$$

noting that e_{ss} is the steady-state output of the phase error detector and ϕ_{ss} is the steady-state value of the phase error process $\phi(k)$ as defined in (3.9).

As shown in Figure 8.3, for $K_1 = 1$ the lock range can *approximately* be determined from the left-hand side of the above inequality.

The instantaneous frequency of the above single-tone PM signal $x(t)$ is given by [65]

$$\omega_i(t) = d[\phi(t)]/dt = \omega_o + \beta\omega_m \cos(\omega_m t) \tag{8.5}$$

where the maximum and the minimum frequencies are given by $\omega_o \pm \beta\omega_m$. Using (8.5) and the above discussion we can find the conditions for demodulating the single-tone PM as follows

$$\beta\omega_m/\omega_o \ < \ 1/3. \tag{8.6}$$

If a similar PM demodulation technique is implemented using the conventional DTL, a dynamic range as in (8.6) will be obtained. It is evident that, despite the reduced structure, TDTL has a performance similar to that of the DTL in many aspects. The above dynamic range in TDTL and CDTL for PM demodulation is much wider than the limit of $\beta\omega_m/\omega_o \ < \ 1/(2\pi+1) \approx 0.13$ obtained for the sinusoidal DPLL in [50], [38].

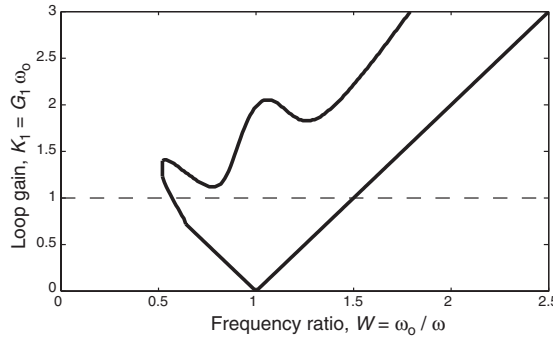


Figure 8.3: Lock range of the TDTL for $\psi_o = \pi/2$.

From Chapter 2, the steady state phase error at the output of the PED can be given by:

$$e_{ss} = h_\psi(\phi_{ss}) = f\left[\mathrm{Tan}^{-1}\left(\frac{\sin(\phi_{ss})}{\sin(\phi_{ss}+\psi)}\right)\right] = \frac{\Lambda_o}{K_1^{'}}$$

where

$$|\Lambda_o/K_1^{'}| < \pi$$

from which the steady-state phase error ϕ_{ss} is given by 3.33) as follows

$$\phi_{ss} = \begin{cases} \alpha & \rho\sin(\lambda) \geq 0 \\ f(\alpha+\pi) & \text{otherwise.} \end{cases} \tag{8.7}$$

where

$$\lambda = \Lambda_o/K_1^{'}$$

and

$$\rho = \frac{\sin(\psi)}{\cot(\lambda)-\cos(\psi)} = \frac{\sin(\psi_o/W)}{\cot(\lambda)-\cos(\psi_o/W)}$$

$$\alpha = \tan^{-1}(\rho)$$

noting that $\tan^{-1}(.)$ is the ordinary arctan function over$(-\pi/2, \pi/2)$. From eqs.(8.5) and the above discussion, the PED output phase in the case of tone-PM demodulation will range between $e_{ss}|_{\max}$ and $e_{ss}|_{\min}$ as follows

$$e_{ss}\Big|_{\max} = \frac{\Lambda_o}{K_1^{'}}\Big|_{\max} = \frac{T_o}{G_1}\Big[1 - \frac{1}{1+\beta\omega_m/\omega_o}\Big] \tag{8.8}$$

$$e_{ss}\Big|_{\min} = \frac{\Lambda_o}{K_1'}\Big|_{\min} = -\frac{T_o}{G_1}\left[\frac{1}{1-\beta\omega_m/\omega_o} - 1\right]. \tag{8.9}$$

The above results are generally true as long as the carrier frequency f_o is much higher than the message maximum frequency f_m such that an approximate locking can occur. This is the case in practical PM and FM transmission systems.

8.2 Performance in Gaussian Noise

We now consider the performance of the above PM demodulator in additive Gaussian noise (AWGN) environment. In Chapter 4 we have shown that if the input signal is affected by AWGN as follows:

$$y(t) = A\sin[\omega_o t + \theta(t)] + n(t) \tag{8.10}$$

where $n(t)$ is additive Gaussian noise with zero mean and variance σ_n^2, then the output of the PED, ξ, can be expressed as follows

$$\xi = e + \eta \tag{8.11}$$

where $e = h_\psi(\phi)$ is the deterministic output phase and η is a non-Gaussian phase noise with zero mean. The sampling index k is removed for simplicity. The pdf of the phase noise η was given in Chapter 4 as follows:

$$\begin{aligned}\rho_{\psi,e}(\eta) &= \frac{1}{2\pi}\exp(-m_{\psi,e}\alpha) + \sqrt{\frac{m_{\psi,e}\alpha}{\pi}}\cos(\eta) \\ &\quad \times \exp[-m_{\psi,e}\alpha\sin^2(\eta)] \\ &\quad \times \left[\frac{1}{2} + \mathrm{erf}\{\sqrt{2m_{\psi,e}\alpha}\cos(\eta)\}\right]\end{aligned}$$

where

$$\begin{aligned}\alpha &= A^2/2\sigma_n^2 \\ \mu_{\psi,\phi} &= \frac{\sin(\psi)}{h_\psi'(\phi)} \\ m_{\psi,e} &= \mu_{\psi,h_\psi^{-1}(e)} \\ \mathrm{erf}(r) &= \frac{1}{\sqrt{2\pi}}\int_0^r e^{-v^2/2}dv.\end{aligned}$$

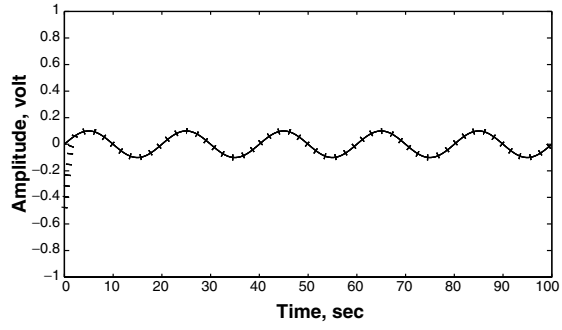


Figure 8.4: Demodulation of a tone-modulated PM signal using the first-order TDTL with $A_m = 1$, $A_o = 1$, $f_o = 1$ Hz, $f_m = 0.05$ Hz, $\beta = 0.1$, $\gamma_o = -0.5$, and $\psi_o = \pi/2$.

When $\psi = \pi/2$, the above pdf reduces to:

$$\begin{aligned} \rho_o(\eta) &= \frac{1}{2\pi}\exp(-\alpha) + \sqrt{\frac{\alpha}{\pi}}\cos(\eta) \times \exp[-\alpha \sin^2(\eta)] \\ &\times \left[\frac{1}{2} + \text{erf}\{\sqrt{2\alpha}\cos(\eta)\}\right]. \end{aligned} \tag{8.12}$$

The variance of ξ is ψ-dependent. In noisy PM demodulation, (8.4) becomes:

$$\begin{aligned} m_o(k) &\approx \frac{1}{\Delta_p}\sum_{i=0}^{k}\xi(k) + \gamma_o \\ &= m(k) + \frac{1}{\Delta_p}\sum_{i=0}^{k}\eta(k) \\ &= m(k) + n_o(k) \end{aligned} \tag{8.13}$$

where

$$n_o(k) = \frac{1}{\Delta_p}\sum_{i=0}^{k}\eta(k). \tag{8.14}$$

The output noise $n_o(k)$ is the sum of several non-Gaussian random variables with zero mean and different values of variance (ψ-dependent). The *Central Limit Theorem* [74] is applicable here, which confirms that $n_o(k)$ is *Gaussian* with zero mean.

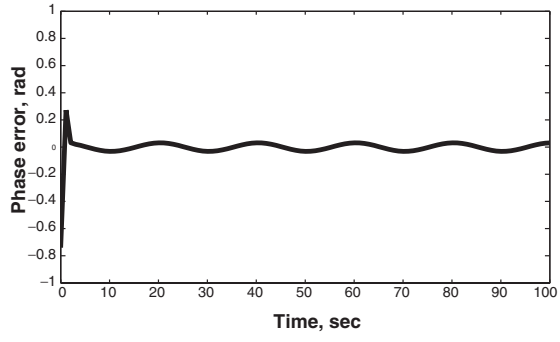


Figure 8.5: Phase error process associated with the demodulation of a tone-modulated PM signal using the first-order TDTL with $A_m = 1$, $A_o = 1$, $f_o = 1$ Hz, $f_m = 0.05$ Hz, $\beta = 0.1$, $\gamma_o = -0.5$, and $\psi_o = \pi/2$.

8.3 Simulation Results

The above system for PM demodulation has been simulated for the following incoming signal:

$$x(t) = A_o \sin[\omega_o t + \beta \sin(\omega_m t) + \gamma_o] \tag{8.15}$$

with $A_m = 1$, $A_o = 1$, $f_o = 1$ Hz, $f_m = 0.05$ Hz, $\beta = 0.1$, $\gamma_o = -0.5$, and $\psi_o = \pi/2$.

Except for a transient disturbance in case of a non-zero initial phase γ_o, the TDTL can efficiently demodulate the information from the carrier as shown in Figure 8.4 and Figure 8.5. The PED output phase error ranges between $e_{ss}|_{\max} = 0.031$ and $e_{ss}|_{\min} = $ -0.031 as per eqs.(8.8) and (8.9).

Figure 8.6 shows the time-domain performance of the above system in the presence of AWGN for SNR = 20 dB. Figure 8.7 shows the performance of the above system in the presence of AWGN for different values of the input (received) signal-to-noise ratios (SNR's) and the modulation index β. The performance is measured in terms of the output SNR ($\mathrm{SNR_o}$) versus the input SNR relation as compared to the case of baseband transmission where the two SNR's are equal. Figure 8.8 shows the performance of the above system versus analog PM demodulation in which the output SNR is related to the input SNR (or baseband SNR, $\mathrm{SNR_b}$) as follows [79]:

$$\mathrm{SNR_o} = \beta^2 P_m \mathrm{SNR_b}. \tag{8.16}$$

where $P_m = p_m/M^2$ is the message power p_m normalized with respect to $M^2 = [\max(m(t))]^2$, given by 1/2 for a tone PM. It is evident that the TDTL-based

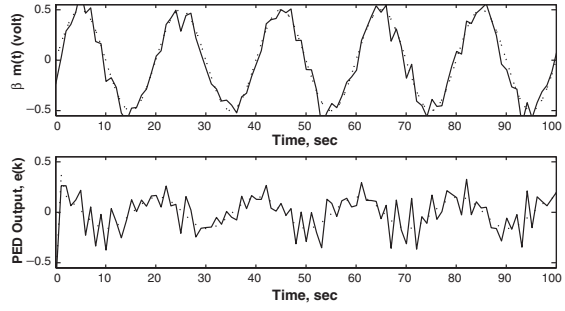


Figure 8.6: TDTL demodulation for noisy tone PM signal with $A_m = 1$, $A_o = 1$, $f_o = 1$ Hz, $f_m = 0.05$ Hz, $\gamma_o = -0.5$ rad, $\psi_o = \pi/2$, and $\beta = 0.5$ and received SNR = 20 dB. Dotted curves are for the noiseless case.

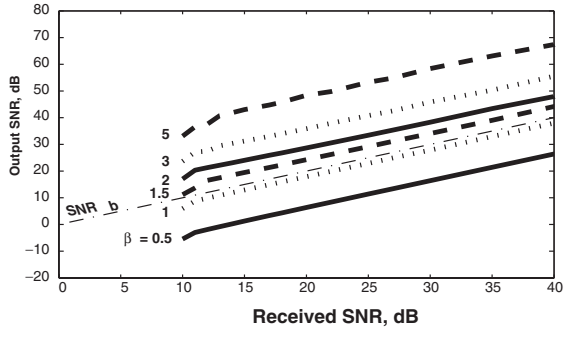


Figure 8.7: Performance of TDTL for noisy tone PM demodulation with $A_m = 1$, $A_o = 1$, $f_o = 1$ Hz, $f_m = 0.05$ Hz, $\gamma_o = 0$, $\psi_o = \pi/2$, and different values for β. The dotted line labelled as SNR_b is for baseband transmission.

PM demodulation outperforms analog demodulation techniques by nearly 20 dB.

8.4 FSK and FM Demodulation

This section demonstrates the results of utilizing the TDTL for the demodulation of FSK and FM signals. For these applications, the first-order loop is more suitable than the second-order one. This is due to the fact that the output level of the phase error is preserved during frequency changes, since the loop will always converge to a nonzero steady-state phase error. This is not the case

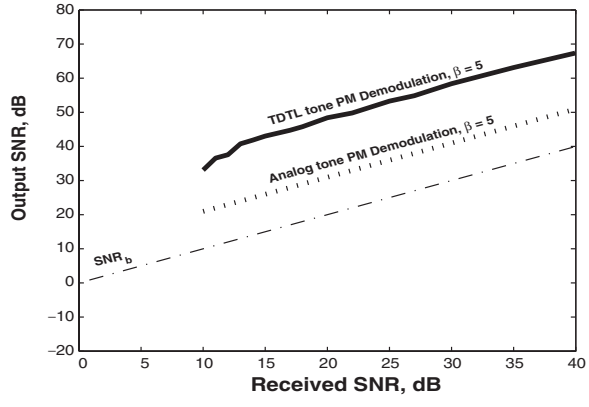


Figure 8.8: Performance of TDTL demodulation versus analog demodulation for noisy tone PM signal with $A_m = 1$, $A_o = 1$, $f_o = 1$ Hz, $f_m = 0.05$ Hz, $\gamma_o = 0$, $\psi_o = \pi/2$, and $\beta = 5$. The dotted line labelled as SNR_b is for baseband transmission.

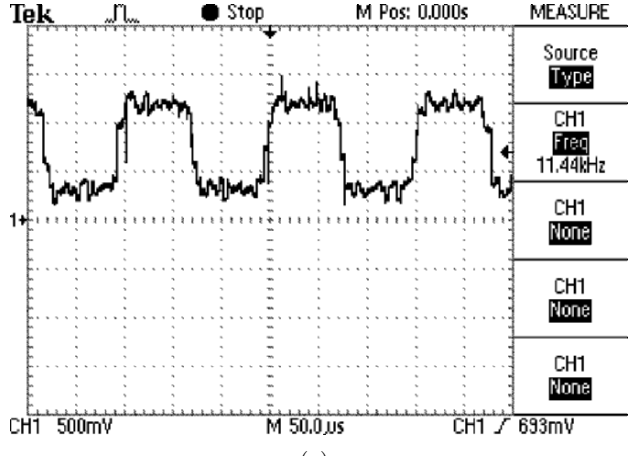
in the second-order loop, where each change in frequency results in a decaying impulse at the phase error, i.e., the need for extra circuitry to determine the level of the transmitted bit is prevalent.

Two examples of FSK demodulation application are shown in Figure 8.9 In the first case, the modulating frequencies are chosen as 260 KHz and 280 KHz respectively, and applied to the input of the loop with a bit rate of 13 Kbps. Figure 8.9-a shows the output of the phase detector in response to the FSK input, and it is clear that this output can be sent directly to decision devices without the need for extra circuitry. This fact is also demonstrated by Figure 8.9-b, which shows the demodulated FSK bit stream of an input with a bit rate of 9 Kbps and modulating frequencies of 225 KHz and 275 KHz.

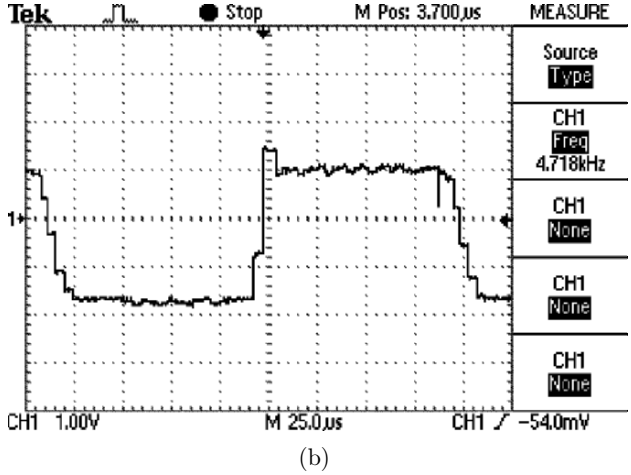
The first-order TDTL can be also utilized for the detection of analogue angle modulated signals. A testing scenario was depicted, where a 10 KHz sinusoidal signal is used to frequency-modulate a carrier of 250 KHz. The FM input is then applied to the TDTL and the base-band sinusoid is recovered from the phase detector as shown in Figure 8.10.

8.5 Wideband FM Signal Detection

The second-order TDTL and the adaptive second-order TDTL were used in the detection of wideband FM signals. Figure 8.11-a and Figure 8-12a show the outputs of the two loops when FM input signal with $\beta = 7$ was applied. The



(a)



(b)

Figure 8.9: FSK demodulation using the first-order TDTL. (a) Bit rate of 13 Kbps. (b) Bit rate of 9 Kbps.

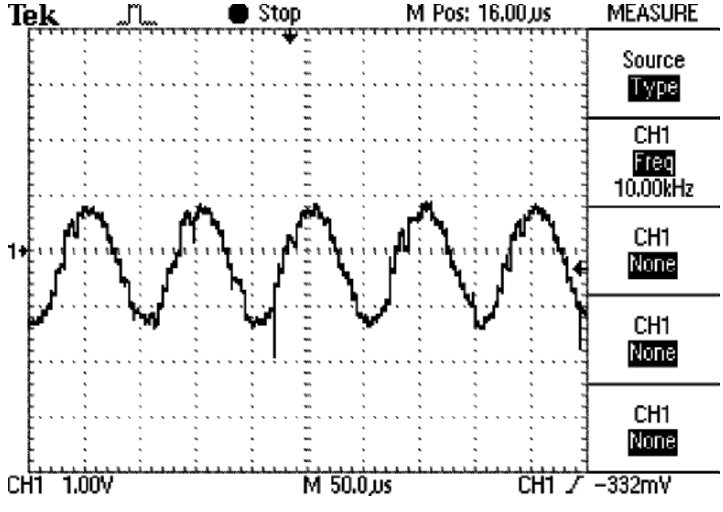


Figure 8.10: FM demodulation using the first-order TDTL.

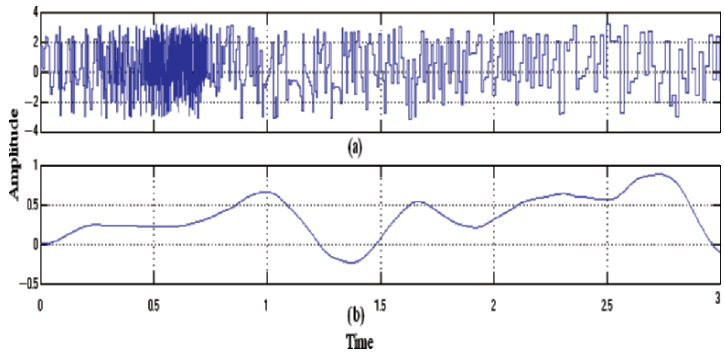


Figure 8.11: Second-order TDTL response for wideband FM signal: (a) non-filtered (b) filtered.

ripples were smoothed using a smoothing filter. The outputs of the two TDTL systems after the smoothing filters are illustrated in Figure 8.11-b and Figure 8.12-b. It can be clearly seen that the adaptive second-order TDTL is much better at detecting the applied wideband FM signal than the basic one.

8.6 Conclusions

This chapter has presented some selected applications of the TDTL. Most importantly, it has been shown that the time-delay digital tanlock loop (TDTL) is capable of demodulating PM (and hence FM) signals in additive Gaussian noise. The basic idea was approximating the non-linear characteristic function of the loop phase error detector (and hence the system equation) under a specific arrangement of the nominal phase-shift to be a right angle. It is shown that the performance of the TDTL as a PM demodulator is comparable to that of the conventional digital tan lock loop (DTL) and is nearly 20-dB better in performance than analog PM demodulators.

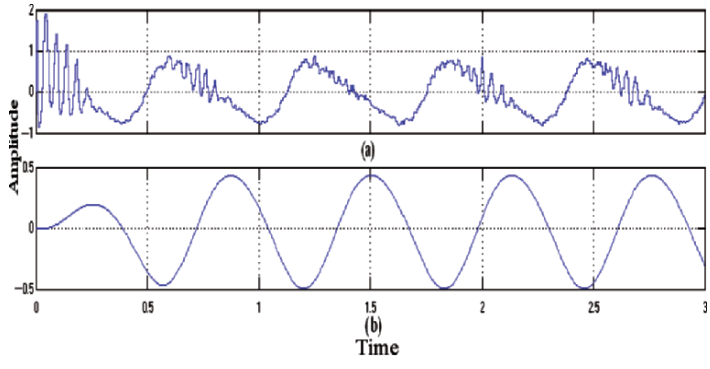


Figure 8.12: Adaptive second-order TDTL response for wideband FM signal: (a) non-filtered (b) filtered.

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